

MACH 5 CPLD Family

Fifth Generation MACH Architecture

FEATURES

- **High logic densities and I/Os for increased logic integration**
  - — 128 to 512 macrocell densities
  - — 68 to 256 I/Os
- **Wide selection of density and I/O combinations to support most application needs**
  - — 6 macrocell density options
  - — 7 I/O options
  - — Up to 4 I/O options per macrocell density
  - — Up to 5 density & I/O options for each package
- **Performance features to fit system needs**
  - — 5.5 ns t_{PD} Commercial, 7.5 ns t_{PD} Industrial
  - — 182 MHz f_{CNT}
  - — Four programmable power/speed settings per block
- **Flexible architecture facilitates logic design**
  - — Multiple levels of switch matrices allow for performance-based routing
  - — 100% routability and pin-out retention
  - — Synchronous and asynchronous clocking, including dual-edge clocking
  - — Asynchronous product- or sum-term set or reset
  - — 16 to 64 output enables
  - — Functions of up to 32 product terms
- **Advanced capabilities for easy system integration**
  - — 3.3-V & 5-V JEDEC-compliant operations
  - — IEEE 1149.1 compliant for boundary scan testing
  - — 3.3-V & 5-V in-system programmable via IEEE 1149.1 Boundary Scan Test Access Port
  - — PCI compliant (-5/-6/-7/-10/-12 speed grades)
  - — Safe for mixed supply voltage system design
  - — Bus-Friendly™ Inputs & I/Os
  - — Individual output slew rate control
  - — Hot socketing
  - — Programmable security bit
- **Advanced E^2CMOS process provides high performance, cost effective solutions**
- **Supported by ispDesignEXPERT™ software for rapid logic development**
  - — Supports HDL design methodologies with results optimized for MACH 5 devices
  - — Flexibility to adapt to user requirements
  - — Software partnerships that ensure customer success
- **Lattice and Third-party hardware programming support**
  - — LatticePRO™ software for in-system programmability support on PCs and Automated Test Equipment
  - — Programming support on all major programmers including Data I/O, BP Microsystems, Advin, and System General

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Table 1. MACH 5 Device Features [1]

Feature	M5-128/1 M5LV-128		M5-192/1	M5-256/1 M5LV-256		M5-320 M5LV-320		M5-384 M5LV-384		M5-512 M5LV-512	
Supply Voltage (V)	5	3.3	5	5	3.3	5	3.3	5	3.3	5	3.3
Macrocells	128	128	192	256	256	320	320	384	384	512	512
Maximum User I/O Pins	120	120	120	160	160	192	192	160	192	256	256
t_{PD} (ns)	5.5	5.5	5.5	5.5	5.5	6.5[2]	6.5[2]	6.5[2]	6.5[2]	6.5[2]	6.5[2]
t_{SS} (ns)	3.0	3.0	3.0	3.0	3.0	3.0[2]	3.0[2]	3.0[2]	3.0[2]	3.0[2]	3.0[2]
t_{COS} (ns)	4.5	4.5	4.5	4.5	4.5	5.0[2]	5.0[2]	5.0[2]	5.0[2]	5.0[2]	5.0[2]
f_{CNT} (MHz)	182	182	182	182	182	167[2]	167[2]	167[2]	167[2]	167[2]	167[2]
Typical Static Power (mA)	35	35	45	55	55	70	70	75	75	100	100
IEEE 1149.1 Boundary Scan Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PCI-Compliant	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Note:

1. *"M5-xxx" is for 5-V devices. "M5LV-xxx" is for 3.3-V devices.*
2. *Preliminary specifications for new 6.5ns (Tpd) speed grade. 7.5ns speed grade in production now.*

GENERAL DESCRIPTION

The MACH® 5 family consists of a broad range of high-density and high-I/O Complex Programmable Logic Devices (CPLDs). The fifth-generation MACH architecture yields fast speeds at high CPLD densities, low power, and supports additional features such as in-system programmability, Boundary Scan testability, and advanced clocking options (Table 1). The MACH 5 family offers 5-V (M5-xxx) and 3.3-V (M5LV-xxx) operation.

Manufactured in state-of-the-art ISO 9000 qualified fabrication facilities on E^2CMOS process technologies, MACH 5 devices are available with pin-to-pin delays as fast as 5.5 ns (Table 2). The 5.5, 6.5, 7.5, 10, and 12-ns devices are compliant with the *PCI Local Bus Specification*.



Table 2. MACH 5 Speed Grades

Device	Speed Grade[1]						
	-5	-6	-7	-10	-12	-15	-20
M5-128[2]			C	C, I	C, I	C, I	I
M5-128/1	C		C, I	C, I	C, I	C, I	I
M5LV-128	C		C,I	C, I	C, I	I	
M5-192/1	C		C, I	C, I	C, I	C, I	I
M5-256[2]			C	C, I	C, I	C, I	I
M5-256/1	C		C, I	C, I	C, I	C, I	I
M5LV-256	C		C, I	C, I	C, I	I	
M5-320		C	C, I	C, I	C, I	C, I	I
M5LV-320		C	C, I	C, I	C, I	C, I	I
M5-384		C[3]	C, I[3]	C, I	C, I	C, I	I
M5LV-384		C[3]	C, I[3]	C, I	C, I	C, I	I
M5-512		C[3]	C, I[3]	C, I	C, I	C, I	I
M5LV-512		C[3]	C, I[3]	C, I	C, I	C, I	I

Note:
1. *C = Commercial grade, I = Industrial grade*
2. */1 version recommended for new designs*
3. *Preliminary specificatons*

With Lattice's unique hierarchical architecture, the MACH 5 family provides densities up to 512 macrocells to support full system logic integration. Extensive routing resources ensure pinout retention as well as high utilization. It is ideal for PAL® block device integration and a wide range of other applications including high-speed computing, low-power applications, communications, and embedded control. At each macrocell density point, Lattice offers several I/O and package options to meet a wide range of design needs (Table 3).

Table 3. MACH 5 Package and I/O Options [1]

	M5-128/1 M5LV-128		M5-192/1	M5-256/1 M5LV-256		M5-320 M5LV-320		M5-384 M5LV-384		M5-512 M5LV-512	
Supply Voltage	**5**	**3.3**	**5**	**5**	**3.3**	**5**	**3.3**	**5**	**3.3**	**5**	**3.3**
100-pin TQFP	68	68, 74	68	68	68*, 74						
100-pin PQFP	68	68*	68*	68*	68						
144-pin TQFP		104			104						
144-pin PQFP	104	104*	104*	104*	104*						
160-pin PQFP	120	120	120	120	120	120*	120	120*	120	120*	120
208-pin PQFP				160	160	160	160	160	160	160	160
240-pin PQFP						184*	184*	184*	184*	184*	184*
256-ball BGA						192	192*	192*	192*	192*	192*
352-ball BGA										256	256

Note:
1. *The I/O options indicated with a "*" are obsolete, please contact factory for more information.*

Advanced power management options allow designers to incrementally reduce power while maintaining the level of performance needed for today's complex designs. I/O safety features allow for mixed-voltage design, and both the 3.3-V and the 5-V device versions are in-system programmable through an IEEE 1149.1 Test Access Port (TAP) interface.

FUNCTIONAL DESCRIPTION

The MACH 5 architecture consists of PAL blocks connected by two levels of interconnect. The **block interconnect** provides routing among 4 PAL blocks. This grouping of PAL blocks joined by the block interconnect is called a **segment**. The second level of interconnect, the **segment interconnect**, ties all of the segments together. The only logic difference between any two MACH 5 devices is the number of segments. Therefore, once a designer is familiar with one device, consistent performance can be expected across the entire family. All devices have four clock pins available which can also be used as logic inputs.

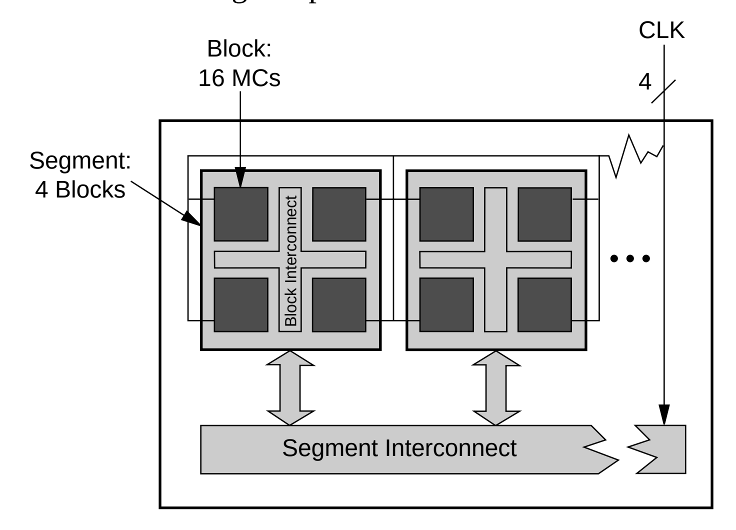


Figure 1. MACH 5 Block Diagram

The MACH 5 PAL blocks consist of the elements listed below (Figure 2). While each PAL block resembles an independent PAL device, it has superior control and logic generation capabilities.

- I/O cells
- Product-term array and Logic Allocator
- Macrocells
- Register control generator
- Output enable generator

I/O Cells

The I/Os associated with each PAL block have a path directly back to that PAL block called **local feedback**. If the I/O is used in another PAL block, the **interconnect feeder** assigns a **block interconnect** line to that signal. The interconnect feeder acts as an input switch matrix. The block and segment interconnects provide connections between any two signals in a device. The **block feeder** assigns block interconnect lines and local feedback lines to the PAL block inputs.

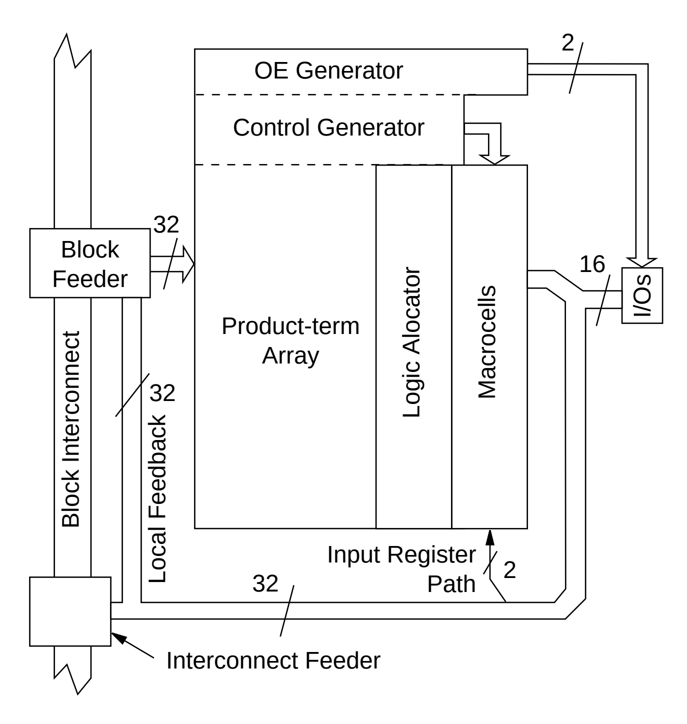


Figure 2. PAL Block Structure

Product-Term Array and Logic Allocator

The product-term array uses the same sum-of-products architecture as PAL devices and consists of 32 inputs (plus their complements) and 64 product terms arranged in 16 **clusters**. A cluster is a sum-of-products function with either 3 of 4 product terms.

Logic allocators assign the clusters to macrocells. Each macrocell can accept up to eight clusters of three or four product terms, but a given cluster can only be steered to one macrocell (Table 4). If only three product terms in a cluster are steered, the fourth can be used as an input to an XOR gate for separate logic generation and/or polarity control.

The **wide logic allocator** is comprised of all 16 of the individual logic allocators and acts as an output switch matrix by reassigning logic to macrocells to retain pinout as designs change. The logic allocation scheme in the MACH 5 device allows for the implementation of large equations (up to 32 product terms) with only one pass through the logic array.

Table 4. Product Term Steering Options for PT Clusters and Macrocells

Macrocell	Available Clusters	Macrocell	Available Clusters
M_0	C_0, C_1, C_2, C_3, C_4	M_8	$C_5, C_6, C_7, C_8, C_9, C_{10}, C_{11}, C_{12}$
M_1	$C_0, C_1, C_2, C_3, C_4, C_5$	M_9	$C_6, C_7, C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}$
M_2	$C_0, C_1, C_2, C_3, C_4, C_5, C_6$	M_{10}	$C_7, C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}$
M_3	$C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7$	M_{11}	$C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$
M_4	$C_0, C_1, C_2, C_3, C_4, C_5, C_6, C_7$	M_{12}	$C_8, C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$
M_5	$C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8$	M_{13}	$C_9, C_{10}, C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$
M_6	$C_2, C_3, C_4, C_5, C_6, C_7, C_8, C_9$	M_{14}	$C_{10}, C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$
M_7	$C_3, C_4, C_5, C_6, C_7, C_8, C_9, C_{10}$	M_{15}	$C_{11}, C_{12}, C_{13}, C_{14}, C_{15}$

Macrocells

The macrocells for MACH 5 devices consist of a storage element which can be configured for combinatorial, registered or latched operation (Figure 3). The D-type flip-flops can be configured as T-type, J-K, or S-R operation through the use of the XOR gate associated with each macrocell.

Each PAL block has the capability to provide two input registers by using macrocells 0 and 15. In order to use this option, these macrocells must be accessed via the I/O pins associated with macrocells 3 and 12, respectively. Once the macrocell is used as an input register, it cannot be used for logic, so its clusters can be re-directed through the logic allocator to another macrocell. The I/O pins associated with macrocells 0 and 15 can still be used as input pins. Although the I/O pins for macrocells 3 and 12 are used to connect to the input registers, these macrocells can still be used as "buried" macrocells to drive device logic via the matrix.

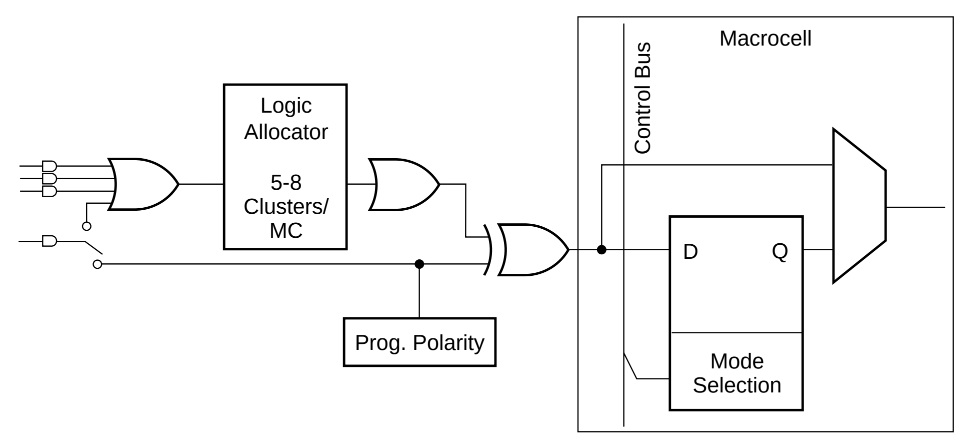


Figure 3. Macrocell Diagram

Control Generator

The control generator provides four configurable clock lines and three configurable set/reset lines to each macrocell in a PAL block. Any of the four clock lines and any of the three set/reset lines can be independently selected by any flip-flop within a block. The clock lines can be configured to provide synchronous global (pin) clocks and asynchronous product term clocks, sum term clocks, and latch enables (Figure 4). Three of the four global clocks, as well as two product-term clocks and one sum-term clock, are available per PAL block. Positive or negative edge clocking is available as well as advanced clocking features such as **complementary** and **biphase** clocking. Complementary clocking provides two clock lines exactly 180 degrees out of phase, and is useful in applications such as fast data paths. A biphase clock line clocks flip-flops on both the positive and negative edges of the clock. The configuration options for the four clock lines per PAL block are as follows:

Clock Line 0 Options

- Global clock (0, 1, 2, or 3) with positive or negative edge clock enable
- Product-term clock (A*B*C)
- Sum-term clock (A+B+C)

Clock Line 1 Options

- ◆ Global clock (0, 1, 2, or 3) with positive edge clock enable
- ◆ Global clock (0, 1, 2, or 3) with negative edge clock enable
- ◆ Global clock (0, 1, 2, or 3) with positive and negative edge clock enable (biphase)

Clock Line 2 Options

- ◆ Global clock (0, 1, 2, or 3) with clock enable

Clock Line 3 Options

- ◆ Complement of clock line 2 (same clock enable)
- ◆ Product-term clock (if clock line 2 does not use clock enable

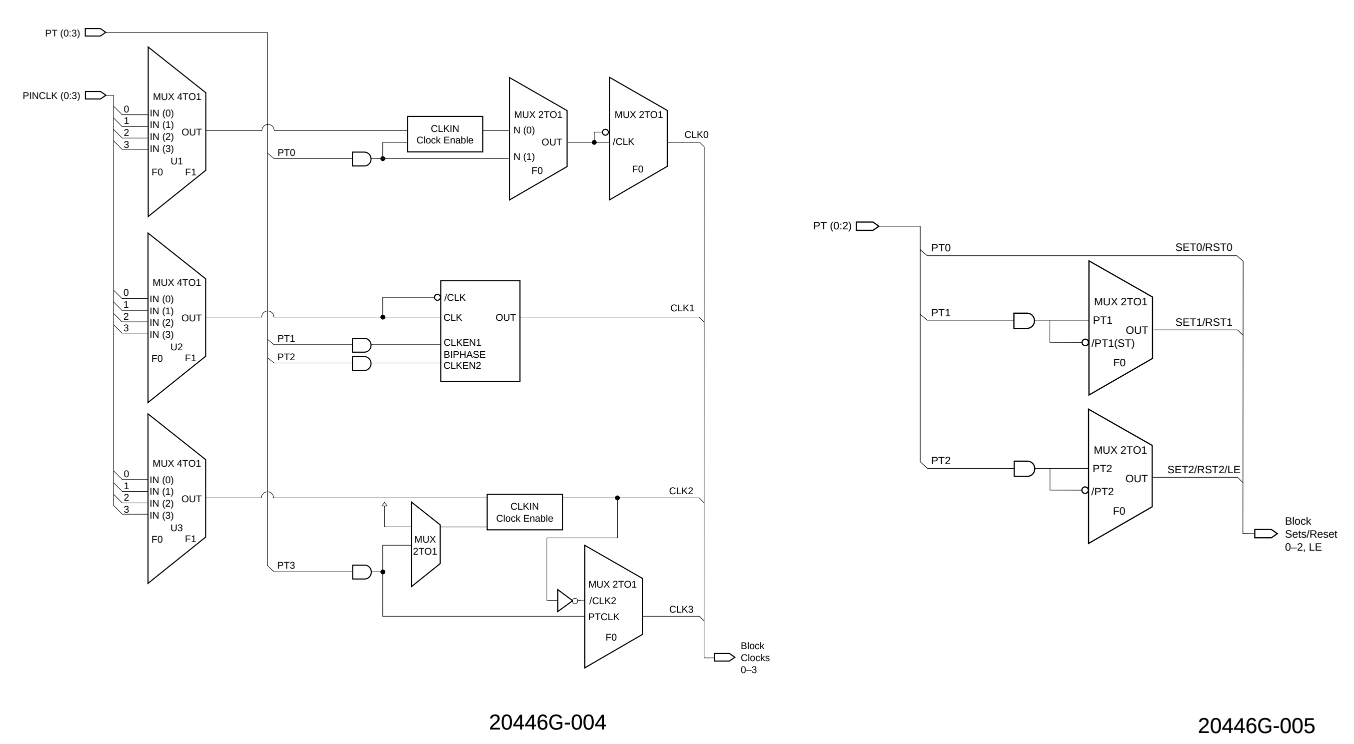


Figure 4. Clock Generator

Figure 5. Set/Reset Generator

The set/reset generation portion of the control generator (Figure 5) creates three set/reset lines for the PAL block. Each macrocell can choose one of these three lines or choose no set/reset at all. All three lines can be configured for product term set/reset and two of the three lines can be configured as sum term set/reset and one of the lines can be configured as product-term or sum-term latch enable. While the set/reset signals are generated in the control generator, whether that signal sets or resets a flip-flop is determined within the individual macrocell. The same signal can set one flip-flop and reset another. PT2 or /PT2 can also be used as a latch enable for macrocells configured as latches.



OE Generator

There is one output enable (OE) generator per PAL block that generates two product-term driven output enables. Each I/O cell is simply an output buffer. Each I/O cell within the PAL block can choose to be permanently enabled, permanently disabled, or choose one of the two product term output enables per PAL block (Figure 6).

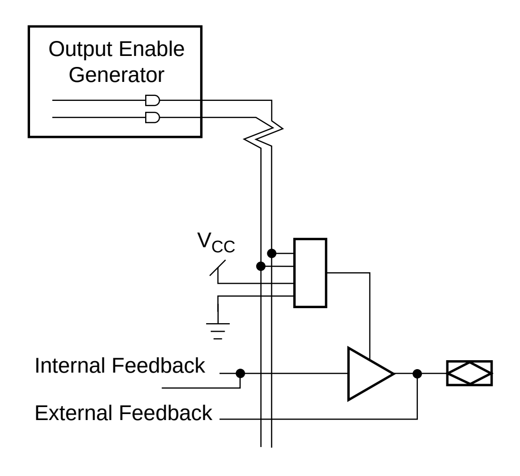


Figure 6. Output Enable Generator and I/O Cell



MACH 5 TIMING MODEL

The primary focus of the MACH 5 timing model is to accurately represent the timing in a MACH 5 device, and at the same time, be easy to understand. This model accurately describes all combinatorial and registered paths through the device, making a distinction between **internal feedback** and **external feedback**. A signal uses internal feedback when it is fed back into the switch matrix or block without having to go through the output buffer. The input register specifications are also reported as internal feedback. When a signal is fed back into the switch matrix after having gone through the output buffer, it is using external feedback.

The parameter, t_{BUF}, is defined as the time it takes to go through the output buffer to the I/O pad. If a signal goes to the internal feedback rather than to the I/O pad, the parameter designator is followed by an “i”. By adding t_{BUF} to this internal parameter, the external parameter is derived. For example, $t_{PD} = t_{PDi} + t_{BUF}$. A diagram representing the modularized MACH 5 timing model is shown in Figure 7. Refer to the Technical Note entitled *MACH 5 Timing and High Speed Design* for a more detailed discussion about the timing parameters.

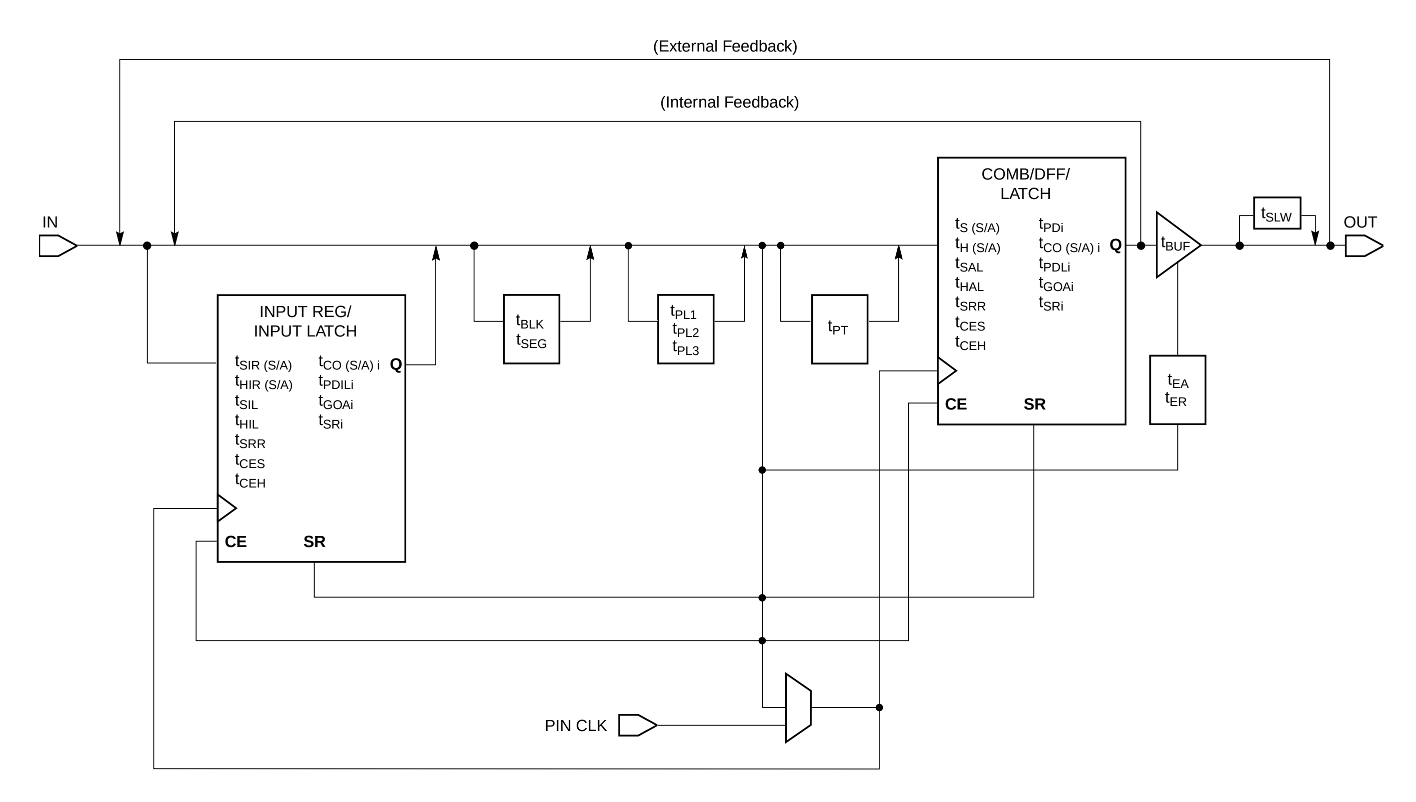


Figure 7. MACH 5 Timing Model



MULTIPLE I/O AND DENSITY OPTIONS

The MACH 5 family offers six macrocell densities in a number of I/O options. This allows designers to choose a device close to their logic density and I/O requirements, thus minimizing costs. For the same package type, every density has the same pin-out. With proper design considerations, a design can be moved to a higher or lower density part as required.

IEEE 1149.1 - COMPLIANT BOUNDARY SCAN TESTABILITY

Most MACH 5 devices have boundary scan registers and are compliant to the IEEE 1149.1 standard. This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test node data to be captured and shifted out for verification. In addition, these devices can be linked into a board-level serial scan path for more complete board-level testing.

IEEE 1149.1 - COMPLIANT IN-SYSTEM PROGRAMMING

Programming devices in-system provides a number of significant benefits including: rapid prototyping, lower inventory levels, higher quality, and the ability to make in-field modifications. All MACH 5 devices provide in-system programming (ISP) capability through their IEEE 1149.1-compliant Boundary Scan Test Access Port. By using the IEEE 1149.1-compliant Boundary Scan Test Access Port as the communication interface through which ISP is achieved, customers get the benefit of a standard, well-defined interface.

MACH 5 devices can be programmed across the commercial temperature and voltage range. The PC-based LatticePRO software facilitates in-system programming of MACH 5 devices. LatticePRO software takes the JEDEC file output produced by design implementation software, along with information about the Boundary Scan chain, and creates a set of vectors that are used to drive the Boundary Scan chain. LatticePRO software can use these vectors to drive a Boundary Scan chain via the parallel port of a PC. Alternatively, LatticePRO software can output files in formats understood by common automated test equipment. This equipment can then be used to program MACH 5 devices during the testing of a circuit board.

PCI COMPLIANT

MACH 5 devices in the -5/-6/-7/-10/-12 speed grades are compliant with the *PCI Local Bus Specification* version 2.1, published by the PCI Special Interest Group (SIG). The 5-V devices are fully PCI-compliant. The 3.3-V devices are mostly compliant but do not meet the PCI condition to clamp the inputs as they rise above V_{CC} because of their 5-V input tolerant feature. MACH 5 devices provide the speed, drive, density, output enables and I/Os for the most complex PCI designs.

SAFE FOR MIXED SUPPLY VOLTAGE SYSTEM DESIGNS [1]

Both the 3.3-V and 5-V V_{CC} MACH 5 devices are safe for mixed supply voltage system designs. The 5-V devices will not overdrive 3.3-V devices above the output voltage of 3.3 V, while they accept inputs from other 3.3-V devices. The 3.3-V devices will accept inputs up to 5.5 V. Both the 3.3-V and 5-V versions have the same high-speed performance and provide easy-to-use mixed-voltage design capability.

Note:

1. *Excludes original M5-128, M5-192, and M5-256 while M5-128/1, M3-192/1 and M5-256/1 are supported. Please refer to Application Note titled "Hot Socketing and Mixed Supply Design with MACH 4 and MACH 5 Devices".*

BUS-FRIENDLY INPUTS AND I/OS

All MACH 5 devices have inputs and I/Os which feature the Bus-Friendly circuitry incorporating two inverters in series which loop back to the input. This double inversion weakly holds the input at its last driven logic state. While it is a good design practice to tie unused pins to a known state, the Bus-Friendly input structure pulls pins away from the input threshold voltage where noise can cause high-frequency switching. At power-up, the Bus-Friendly latches are reset to a logic level "1." For the circuit diagram, please refer to the document entitled *MACH Endurance Characteristics* on the Lattice Data Book CD-ROM or Lattice web site.

POWER MANAGEMENT

There are 4 power/speed options in each MACH 5 PAL block (Table 5). The speed and power tradeoff can be tailored for each design. The signal speed paths in the lower-power PAL blocks will be slower than those in the higher-power PAL blocks. This feature allows speed critical paths to run at maximum frequency while the rest of the signal paths operate in a lower-power mode. In large designs, there may be several different speed requirements for different portions of the design.

Table 5. Power Levels

High Speed/High Power	100% Power
Medium High Speed/Medium High Power	67% Power
Medium Low Speed/Medium Low Power	40% Power
Low Speed/Low Power	20% Power

PROGRAMMABLE SLEW RATE

Each MACH 5 device I/O has an individually programmable output slew rate control bit. Each output can be individually configured for the higher speed transition (3 V/ns) or for the lower noise transition (1 V/ns). For high-speed designs with long, unterminated traces, the slow-slew rate will introduce fewer reflections, less noise, and keep ground bounce to a minimum. For designs with short traces or well terminated lines, the fast slew rate can be used to achieve the highest speed. The slew rate is adjusted independent of power.

POWER-UP RESET/SET

All flip-flops power up to a known state for predictable system initialization. If a macrocell is configured to SET on a signal from the control generator, then that macrocell will be SET during device power-up. If a macrocell is configured to RESET on a signal from the control generator or is not configured for set/reset, then that macrocell will RESET on power-up. To guarantee



initialization values, the V_{CC} rise must be monotonic and the clock must be inactive until the reset delay time has elapsed.

SECURITY BIT

A programmable security bit is provided on the MACH 5 devices as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors. Programming and verification are also defeated by the security bit. The bit can only be reset by erasing the entire device.

MACH 5 PAL BLOCK

Output Enable
Output Enable
Switch Matrix
Logic Allocator
C_0 … C_{15}
M_0 … M_{15}
Macro cell
I/O Cell
I/O
Control Generator
CLK
0 4 8 12 16 20 24 28 32 36 40 44 48 52 56 60 63

20446G-015



BLOCK DIAGRAM — M5(LV)-128/XXX

SEGMENT 0

Block A/Macrocells 0-15

Block D/Macrocells 0-15

I/O Cells

Macrocells

Control Generator

64 x 73 AND Logic Array and Logic Allocator

16, 2, 32, 64 PT, 7 PT, 2 PT OE, 7

Block Interconnect

$I_{0, 1}$

Block B/Macrocells 0-15

Block C/Macrocells 0-15

CLK0
CLK1
CLK2
CLK3

S E G M E N T I N T E R C O N N E C T

Block A/Macrocells 0-15

Block D/Macrocells 0-15

Block Interconnect

$I_{2, 3}$

Block B/Macrocells 0-15

Block C/Macrocells 0-15

SEGMENT 1

20446G-007

BLOCK DIAGRAM — M5-192/XXX

SEGMENT 2

SEGMENT 0

SEGMENT 1

SEGMENT INTERCONNECT

CLK0
CLK1
CLK2
CLK3

20446G-008

BLOCK DIAGRAM — M5(LV)-256/XXX

20446G-009

BLOCK DIAGRAM — M5(LV)-320/XXX

20446G-010

BLOCK DIAGRAM — M5(LV)-384/XXX

SEGMENT 0
SEGMENT 5
SEGMENT 4
SEGMENT INTERCONNECT
SEGMENT 1
SEGMENT 2
SEGMENT 3

Block A/Macrocells 0-15
Block B/Macrocells 0-15
Block C/Macrocells 0-15
Block D/Macrocells 0-15
Block Interconnect
I/O Cells
Macrocells
Control Generator
64 x 73 AND Logic Array and Logic Allocator
64 PT
7 PT
2 PT OE
CLK0
CLK1
CLK2
CLK3

20446G-011

BLOCK DIAGRAM — M5(LV)-512/XXX

Continued

20446G-012

BLOCK DIAGRAM — M5(LV)-512/XXX

SEGMENT 5

SEGMENT 6

SEGMENT 4

SEGMENT 3

Block A/Macrocells 0-15

Block B/Macrocells 0-15

Block C/Macrocells 0-15

Block D/Macrocells 0-15

Block Interconnect

I/O Cells

Macrocells

Control Generator

64 x 73 AND Logic Array and Logic Allocator

64 PT

7 PT

2 PT OE

16

32

2

7

I_3

I_2

I N T E R C O N N E C T

Continued

20446G-013



ABSOLUTE MAXIMUM RATINGS

M5

Storage Temperature . . . . -65°C to +150°C

Device Junction
Temperature (Note 1) . . . . +130°C or +150°C

Supply Voltage
with Respect to Ground . . . . -0.5 V to +7.0 V

DC Input Voltage . . . . -0.5 V to 5.5 V

Static Discharge Voltage . . . . 2000 V

Latchup Current (-40°C to +85°C) . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . +4.75 V to +5.25 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

5-V DC CHARACTERISITICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (For M5-128/1, M5-192/1, M5-256/1, M5-320, M5-384, M5-512 Devices)	I_{OH} = -3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4			V
		I_{OH} = 0 mA, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL}			3.3	V
	Output HIGH Voltage (For M5-128, M5-192, M5-256 Devices)	I_{OH} = -3.2 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}	2.4			V
		I_{OH} = -2.5 mA, V_{CC} = 5.25 V, V_{IN} = V_{IH} or V_{IL}			3.6	V
V_{OL}	Output LOW Voltage (Note 2)	I_{OL} = +16 mA, V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}			0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25, V_{CC} = Max (Note 4)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0, V_{CC} = Max (Note 4)			-10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)			-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 5)	-30		-180	mA

Note:

1. *150° for M5-128, M5-192 and M5-256 devices. 130° for M5-128/1, M5-192/1, M5-256/1, M5-320, M5-384 and M5-512 devices.*
2. *Total I_{OL} between ground pins should not exceed 64 mA.*
3. *These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.*
4. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.*
5. *Not more than one output should be shorted at a time. Duration of the short-circuit should not exceed one second.*

ABSOLUTE MAXIMUM RATINGS

M5LV

Storage Temperature . . . . -65°C to +150°C

Device Junction Temperature . . . . +130°C

Supply Voltage
with Respect to Ground . . . . -0.5 V to +4.5 V

DC Input Voltage . . . . -0.5 V to 5.5 V

Static Discharge Voltage . . . . 2000 V

Latchup Current (-40°C to +85°C) . . . . 200 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . 0°C to +70°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . +3.0 V to +3.6 V

Industrial (I) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . -40°C to +85°C

Supply Voltage (V_{CC})
with Respect to Ground . . . . +3.0 V to +3.6 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

3.3-V DC CHARACTERISITICS OVER OPERATING RANGES

Parameter Symbol	Parameter Description	Test Description		Min	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = -100 µA	V_{CC} -0.2		V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = 3.2 mA	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min	I_{OL} = 100 µA		0.2	V
		V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA (Note 1)		0.5	V
V_{IH}	Input HIGH Voltage	$V_{OUT} \geq V_{OH}$ Min or $V_{OUT} \leq V_{OL}$ Max (Note 2)		2.0	5.5	V
V_{IL}	Input LOW Voltage	$V_{OUT} \geq V_{OH}$ Min or $V_{OUT} \leq V_{OL}$ Max (Note 2)		-0.3	0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 3.6, V_{CC} = Max (Note 3)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0, V_{CC} = Max (Note 3)			-10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 3.6, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0, V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 3)			-10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} (Note 4)		-15	-160	mA

Notes:

1. *Total I_{OL} between ground pins should not exceed 64 mA.*
2. *These are absolute values with respect to device ground, and all overshoots due to system and/or tester noise are included.*
3. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} or I_{IH} and I_{OZH}.*
4. *Not more than one output should be shorted at one time. Duration of the short-circuit should not exceed one second.*



M5(LV) TIMING PARAMETERS OVER OPERATING RANGES[1]

		-5		-6		-7		-10		-12		-15		-20		
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Combinatorial Delay:																
t_{PDi}	Internal combinatorial propagation delay		3.5		4.5		5.5		8.0		10.0		13.0		18.0	ns
t_{PD}	Combinatorial propagation delay		5.5		6.5		7.5		10.0		12.0		15.0		20.0	ns
Registered Delays:																
t_{SS}	Synchronous clock setup time	3.0		3.0		4.0		5.0		6.0		8.0		10.0		ns
t_{SA}	Asynchronous clock setup time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t_{HS}	Synchronous clock hold time	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HA}	Asynchronous clock hold time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t_{COSi}	Synchronous clock to internal output		2.5		3.0		4.0		5.0		6.0		8.0		10.0	ns
t_{COS}	Synchronous clock to output		4.5		5.0		6.0		7.0		8.0		10.0		12.0	ns
t_{COAi}	Asynchronous clock to internal output		6.0		6.0		8.0		10.0		13.0		15.0		18.0	ns
t_{COA}	Asynchronous clock to output		8.0		8.0		10.0		12.0		15.0		17.0		20.0	ns
Latched Delays:																
t_{SAL}	Latch setup time	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t_{HAL}	Latch hold time	3.0		3.0		4.0		5.0		6.0		7.0		8.0		ns
t_{PDLi}	Transparent latch internal		6.0		7.0		7.0		8.0		9.0		10.0		10.0	ns
t_{PDL}	Propagation delay through transparent latch		8.0		9.0		9.0		10.0		11.0		12.0		12.0	ns
t_{GOAi}	Gate to internal output		7.0		8.0		8.0		9.0		10.0		11.0		12.0	ns
t_{GOA}	Gate to output		9.0		10.0		10.0		11.0		12.0		13.0		14.0	ns
Input Register Delays:																
t_{SIRS}	Input register setup time using a synchronous clock	2.0		2.0		2.0		3.0		3.0		3.0		3.0		ns
t_{SIRA}	Input register setup time using an asynchronous clock	0.0		0.0		0.0		0.0		0.0		0.0		0.0		ns
t_{HIRS}	Input register hold time using a synchronous clock	3.0		3.0		3.0		4.0		4.0		4.0		4.0		ns
t_{HIRA}	Input register hold time using an asynchronous clock	6.0		6.0		6.0		7.0		7.0		7.0		7.0		ns
Input Latch Delays:																
t_{SIL}	Input latch setup time	2.0		2.0		2.0		3.0		3.0		3.0		3.0		ns
t_{HIL}	Input latch hold time	6.0		6.0		6.0		7.0		7.0		7.0		7.0		ns
t_{PDILi}	Transparent input latch		5.0		5.0		5.5		6.0		6.0		6.0		6.0	ns
Output Delays:																
t_{BUF}	Output buffer delay		2.0		2.0		2.0		2.0		2.0		2.0		2.0	ns
t_{SLW}	Slow slew rate delay		2.5		2.5		2.5		2.5		2.5		2.5		2.5	ns
t_{EA}	Output enable time		7.5		7.5		9.5		10.0		12.0		15.0		20.0	ns
t_{ER}	Output disable time		7.5		7.5		9.5		10.0		12.0		15.0		20.0	ns



M5(LV) TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUED)

		-5		-6		-7		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Power Delays:																
t_{PL1}	Power level 1 delay (Note 2)		4.0 (5.0)		4.0		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)		4.0 (5.0)	ns
t_{PL2}	Power level 2 delay (Note 2)		6.0 (9.0)		6.0		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)		6.0 (9.0)	ns
t_{PL3}	Power level 3 delay (Note 2)		9.0 (17.5)		9.0		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)		9.0 (17.5)	ns
Additional Cluster Delay:																
t_{PT}	Product term cluster delay		0.3		0.3		0.3		0.3		0.3		0.3		0.3	ns
Interconnect Delays:																
t_{BLK}	Block interconnect delay		1.5		1.5		1.5		2.0		2.0		2.0		2.0	ns
t_{SEG}	Segment interconnect delay		4.5		4.5		5.0		6.0		6.0		6.0		6.0	ns
Reset and Preset Delays:																
t_{SRi}	Asynchronous reset or preset to internal register output		6.0		8.0		8.0		10.0		12.0		14.0		16.0	ns
t_{SR}	Asynchronous reset or preset to register output		8.0		10.0		10.0		12.0		14.0		16.0		18.0	ns
t_{SRR}	Reset and set register recovery time	5.5		7.5		7.5		8.0		9.0		10.0		11.0		ns
t_{SRW}	Asynchronous reset or preset width	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
Clock Enable Delays:																
t_{CES}	Clock enable setup time	4.0		5.0		5.0		6.0		7.0		7.0		8.0		ns
t_{CEH}	Clock enable hold time	3.0		4.0		4.0		5.0		6.0		6.0		7.0		ns
Width:																
t_{WLS}	Global clock width low (Note 3)	2.5		3.0		3.0		4.0		5.0		6.0		6.0		ns
t_{WHS}	Global clock width high (Note 3)	2.5		3.0		3.0		4.0		5.0		6.0		6.0		ns
t_{WLA}	Product term clock width low	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t_{WHA}	Product term clock width high	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t_{GWA}	Gate width low (for low transparent) or high (for high transparent)	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns
t_{WIR}	Input register clock width low or high	3.0		4.0		4.0		5.0		6.0		7.0		8.0		ns

M5(LV) TIMING PARAMETERS OVER OPERATING RANGES[1] (CONTINUED)

		-5		-6		-7		-10		-12		-15		-20		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Frequency:																
f_{MAX}	External feedback, PAL block level. Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COS})$	133		125		100		83.3		71.4		55.6		45.5		MHz
	Internal feedback, PAL block level. Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{COSi})$	182		167		125		100		83.3		62.5		50.0		MHz
	No feedback PAL block level. Min of $1/(t_{WLS} + t_{WHS})$ or $1/(t_{SS} + t_{HS})$	200		167		167		125		100		83.3		83.3		MHz
f_{MAXA}	External feedback, PAL block level. Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COA})$	91		91		71.4		58.8		47.6		41.7		35.7		MHz
	Internal feedback, PAL block level. Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{COAi})$	111		111		83.3		66.7		52.6		45.5		38.5		MHz
	No feedback, PAL block level. Min of $1/(t_{WLA} + t_{WHA})$ or $1/(t_{SA} + t_{HA})$	167		125		125		100		83.3		71.4		62.5		MHz
f_{MAXI}	Maximum input register frequency $1/(t_{SIRS}+t_{HIRS})$ or $1/(2 \times t_{WICW})$	167		125		125		100		83.3		71.4		62.5		MHz

Notes:

1. *See "MACH Switching Test Circuits" documentation on the Lattice Data Book CD-ROM or Lattice web site.*
2. *Numbers in parentheses are for M5-128, M5-192, M5-256.*
3. *If a signal is used as both a clock and a logic array input, then the maximum input frequency applies ($f_{MAX}/2$).*

CAPACITANCE[1]

Parameter Symbol	Parameter Description	Test conditions		Typ	Unit
C_{IN}	I/CLK pin	V_{IN} =2.0 V	3.3 V or 5 V, 25º C, 1 MHz	12	pF
$C_{I/O}$	I/O pin	V_{OUT} =2.0 V	3.3 V or 5 V, 25º C, 1 MHz	10	pF

1. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where these parameters may be affected.*

I_{CC} vs. FREQUENCY

These curves represent the typical power consumption for a particular device at system frequency. The selected “typical” pattern is a 16-bit up-down counter. This pattern fills the device and exercises every macrocell. Maximum frequency shown uses internal feedback and a D-type register. Power/Speed are optimized to obtain the highest counter frequency and the lowest power. The highest frequency (LSBs) is placed in common PAL blocks, which are set to high power. The lowest frequency signals (MSBs) are placed in a common PAL block and set to lowest power. For a more detailed discussion about MACH 5 power consumption, refer to the application note entitled *MACH 5 Power* in the Application Notes section on the Lattice Data Book CD-ROM or Lattice web site.

I_{CC} CURVES AT HIGH /LOW POWER MODES

V_{CC} = 5 V or 3.3 V, T_A = 25º C

M5(LV)-512 high power
M5(LV)-384 high power
M5(LV)-320 high power
M5-256/1 and M5LV-25 high power
M5-192/1 high power
M5-128/1 and M5LV-128 high power
M5(LV)-512 low power
M5(LV)-384 low power
M5(LV)-320 low power
M5-256/1 and M5LV-256 low power
M5-192/1 low power
M5-128/1 and M5LV-128 low power
I_{CC} (mA)
Frequency (MHz)
20446G-048

Figure 8. I_{CC} Curves at High/Low Power Modes



V_{CC} = 5 V, T_A = 25º C

I_{CC} (mA)

700
600
500
400
300
200
100
0

M5-256 high power
M5-192 high power
M5-128 high power
M5-256 low power
M5-192 low power
M5-128 low power

0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150

Frequency (MHz)

20446G-049

Figure 9. I_{CC} Curves at High/Low Power Modes



100-PIN PQFP CONNECTION DIAGRAM

Top View

100-Pin PQFP (68 I/O)

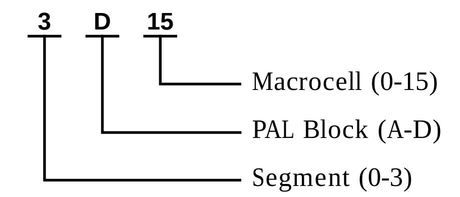
Pin	Signal	M5-256* / M5LV-256	M5-192*	M5-128 / M5LV-128*
1	GND			
2	GND			
3	TDI			
4	I/O0	0A12	0A12	0A14
5	I/O1	0B13	0B13	0B13
6	I/O2	0B12	0B12	0B12
7	I/O3	0B11	0B11	0B11
8	I/O4	0B8	0B8	0B8
9	I/O5	0B7	0B7	0B7
10	I/O6	0B4	0B4	0B4
11	I/O7	0B3	0B3	0B3
12	I/O8	0B2	0B2	0B2
13	I0/CLK0			
14	V_{CC}			
15	V_{CC}			
16	GND			
17	GND			
18	I1/CLK1			
19	I/O9	1B2	1B2	1B2
20	I/O10	1B3	1B3	1B3
21	I/O11	1B4	1B4	1B4
22	I/O12	1B7	1B7	1B7
23	I/O13	1B8	1B8	1B8
24	I/O14	1B11	1B11	1B11
25	I/O15	1B12	1B12	1B12
26	I/O16	1B13	1B13	1B13
27	I/O17	1A12	1A12	1A14
28	TCK			
29	GND			
30	GND			
31	I/O18	1A7	1A7	1A13
32	I/O19	1A6	1A6	1A12
33	I/O20	1A5	1A5	1A11
34	I/O21	1A4	1A4	1A8
35	I/O22	1A3	1A3	1A7
36	I/O23	1A2	1A2	1A4
37	I/O24	1A1	1A1	1A3
38	I/O25	1A0	1A0	1A2
39	V_{CC}			
40	GND			
41	GND			
42	V_{CC}			
43	I/O26	2A0	2D0	1D2
44	I/O27	2A1	2D1	1D3
45	I/O28	2A2	2D2	1D4
46	I/O29	2A3	2D3	1D7
47	I/O30	2A4	2D4	1D8
48	I/O31	2A5	2D5	1D11
49	I/O32	2A6	2D6	1D12
50	I/O33	2A7	2D7	1D13
51	GND			
52	GND			
53	TMS			
54	I/O34	2A12	2D12	1D14
55	I/O35	2B13	2C13	1C13
56	I/O36	2B12	2C12	1C12
57	I/O37	2B11	2C11	1C11
58	I/O38	2B8	2C8	1C8
59	I/O39	2B7	2C7	1C7
60	I/O40	2B4	2C4	1C4
61	I/O41	2B3	2C3	1C3
62	I/O42	2B2	2C2	1C2
63	I2/CLK2			
64	V_{CC}			
65	V_{CC}			
66	GND			
67	GND			
68	I3/CLK3			
69	I/O43	3B2	2B2	0C2
70	I/O44	3B3	2B3	0C3
71	I/O45	3B4	2B4	0C4
72	I/O46	3B7	2B7	0C7
73	I/O47	3B8	2B8	0C8
74	I/O48	3B11	2B11	0C11
75	I/O49	3B12	2B12	0C12
76	I/O50	3B13	2B13	0C13
77	I/O51	3A12	2A12	0D14
78	TDO			
79	GND			
80	GND			
81	I/O52	3A7	2A7	0D13
82	I/O53	3A6	2A6	0D12
83	I/O54	3A5	2A5	0D11
84	I/O55	3A4	2A4	0D8
85	I/O56	3A3	2A3	0D7
86	I/O57	3A2	2A2	0D4
87	I/O58	3A1	2A1	0D3
88	I/O59	3A0	2A0	0D2
89	V_{CC}			
90	GND			
91	GND			
92	V_{CC}			
93	I/O60	0A0	0A0	0A2
94	I/O61	0A1	0A1	0A3
95	I/O62	0A2	0A2	0A4
96	I/O63	0A3	0A3	0A7
97	I/O64	0A4	0A4	0A8
98	I/O65	0A5	0A5	0A11
99	I/O66	0A6	0A6	0A12
100	I/O67	0A7	0A7	0A13

*Package obsolete, contact factory.

20446G-016

Pin Designations

CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out



100-PIN TQFP CONNECTION DIAGRAM – 68 I/O

Top View

100-Pin TQFP (68 I/O)

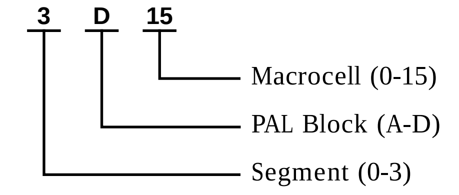
Pin	Signal	M5-256 / M5LV-256*	M5-192	M5-128 / M5LV-128
1	TDI			
2	I/O0	0A12	0A12	0A14
3	I/O1	0B13	0B13	0B13
4	I/O2	0B12	0B12	0B12
5	I/O3	0B11	0B11	0B11
6	I/O4	0B8	0B8	0B8
7	I/O5	0B7	0B7	0B7
8	I/O6	0B4	0B4	0B4
9	I/O7	0B3	0B3	0B3
10	I/O8	0B2	0B2	0B2
11	I0/CLK0			
12	V_{CC}			
13	GND			
14	GND			
15	I1/CLK1			
16	I/O9	1B2	1B2	1B2
17	I/O10	1B3	1B3	1B3
18	I/O11	1B4	1B4	1B4
19	I/O12	1B7	1B7	1B7
20	I/O13	1B8	1B8	1B8
21	I/O14	1B11	1B11	1B11
22	I/O15	1B12	1B12	1B12
23	I/O16	1B13	1B13	1B13
24	I/O17	1A12	1A12	1A14
25	TCK			
26	GND			
27	GND			
28	I/O18	1A7	1A7	1A13
29	I/O19	1A6	1A6	1A12
30	I/O20	1A5	1A5	1A11
31	I/O21	1A4	1A4	1A8
32	I/O22	1A3	1A3	1A7
33	I/O23	1A2	1A2	1A4
34	I/O24	1A1	1A1	1A3
35	I/O25	1A0	1A0	1A2
36	NC			
37	V_{CC}			
38	GND			
39	GND			
40	V_{CC}			
41	I/O26	2A0	2D0	1D2
42	I/O27	2A1	2D1	1D3
43	I/O28	2A2	2D2	1D4
44	I/O29	2A3	2D3	1D7
45	I/O30	2A4	2D4	1D8
46	I/O31	2A5	2D5	1D11
47	I/O32	2A6	2D6	1D12
48	I/O33	2A7	2D7	1D13
49	GND			
50	GND			
51	TMS			
52	I/O34	2A12	2D12	1D14
53	I/O35	2B13	2C13	1C13
54	I/O36	2B12	2C12	1C12
55	I/O37	2B11	2C11	1C11
56	I/O38	2B8	2C8	1C8
57	I/O39	2B7	2C7	1C7
58	I/O40	2B4	2C4	1C4
59	I/O41	2B3	2C3	1C3
60	I/O42	2B2	2C2	1C2
61	I2/CLK2			
62	V_{CC}			
63	GND			
64	I3/CLK3			
65	I/O43	3B2	2B2	0C2
66	I/O44	3B3	2B3	0C3
67	I/O45	3B4	2B4	0C4
68	I/O46	3B7	2B7	0C7
69	I/O47	3B8	2B8	0C8
70	I/O48	3B11	2B11	0C11
71	I/O49	3B12	2B12	0C12
72	I/O50	3B13	2B13	0C13
73	I/O51	3A12	2A12	0D14
74	TDO			
75	GND			
76	GND			
77	I/O52	3A7	2A7	0D13
78	I/O53	3A6	2A6	0D12
79	I/O54	3A5	2A5	0D11
80	I/O55	3A4	2A4	0D8
81	I/O56	3A3	2A3	0D7
82	I/O57	3A2	2A2	0D4
83	I/O58	3A1	2A1	0D3
84	I/O59	3A0	2A0	0D2
85	NC			
86	V_{CC}			
87	GND			
88	GND			
89	V_{CC}			
90	I/O60	0A0	0A0	0A2
91	I/O61	0A1	0A1	0A3
92	I/O62	0A2	0A2	0A4
93	I/O63	0A3	0A3	0A7
94	I/O64	0A4	0A4	0A8
95	I/O65	0A5	0A5	0A11
96	I/O66	0A6	0A6	0A12
97	I/O67	0A7	0A7	0A13
98	NC			
99	GND			
100	GND			

*Package obsolete, contact factory.

20446G-017

Pin Designations

CLK	= Clock	V_{CC}	= Supply Voltage
GND	= Ground	TDI	= Test Data In
I	= Input	TCK	= Test Clock
I/O	= Input/Output	TMS	= Test Mode Select
NC	= No Connect	TDO	= Test Data Out





100-PIN TQFP CONNECTION DIAGRAM – 74 I/O

Top View

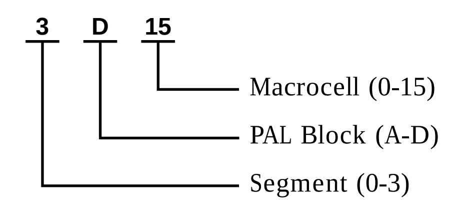
100-Pin TQFP (74 I/O)

Pin	Function	M5LV-256	M5LV-128
1	TDI		
2	I/O0	0A12	0A14
3	I/O1	0B13	0B13
4	I/O2	0B12	0B12
5	I/O3	0B11	0B11
6	I/O4	0B8	0B8
7	I/O5	0B7	0B7
8	I/O6	0B4	0B4
9	I/O7	0B3	0B3
10	I/O8	0B2	0B2
11	I0/CLK0		
12	V_{CC}		
13	GND		
14	GND		
15	I1/CLK1		
16	I/O9	1B2	1B2
17	I/O10	1B3	1B3
18	I/O11	1B4	1B4
19	I/O12	1B7	1B7
20	I/O13	1B8	1B8
21	I/O14	1B11	1B11
22	I/O15	1B12	1B12
23	I/O16	1B13	1B13
24	I/O17	1A12	1A14
25	TCK		
26	GND		
27	I/O18	1A7	1A13
28	I/O19	1A6	1A12
29	I/O20	1A5	1A11
30	I/O21	1A4	1A10
31	I/O22	1A3	1A8
32	I/O23	1A2	1A7
33	I/O24	1A1	1A4
34	I/O25	1A0	1A3
35	I/O26	1D11	1A2
36	1/O27	1D12	1A1
37	V_{CC}		
38	GND		
39	GND		
40	V_{CC}		
41	I/O28	2D12	1D2
42	I/O29	2A0	1D3
43	I/O30	2A1	1D4
44	I/O31	2A2	1D7
45	I/O32	2A3	1D8
46	I/O33	2A4	1D10
47	I/O34	2A5	1D11
48	I/O35	2A6	1D12
49	1/O36	2A7	1D13
50	GND		
51	TMS		
52	I/O37	2A12	1D14
53	I/O38	2B13	1C13
54	I/O39	2B12	1C12
55	I/O40	2B11	1C11
56	I/O41	2B8	1C8
57	I/O42	2B7	1C7
58	I/O43	2B4	1C4
59	I/O44	2B3	1C3
60	I/O45	2B2	1C2
61	I2/CLK2		
62	V_{CC}		
63	GND		
64	I3/CLK3		
65	I/O46	3B2	0C2
66	I/O47	3B3	0C3
67	I/O48	3B4	0C4
68	I/O49	3B7	0C7
69	I/O50	3B8	0C8
70	I/O51	3B11	0C11
71	I/O52	3B12	0C12
72	I/O53	3B13	0C13
73	I/O54	3A12	0D14
74	TDO		
75	GND		
76	GND		
77	I/O55	3A7	0D13
78	I/O56	3A6	0D12
79	I/O57	3A5	0D11
80	I/O58	3A4	0D8
81	I/O59	3A3	0D7
82	I/O60	3A2	0D4
83	I/O61	3A1	0D3
84	I/O62	3A0	0D2
85	I/O63	3D12	0D1
86	V_{CC}		
87	GND		
88	GND		
89	V_{CC}		
90	I/O64	0D12	0A2
91	I/O65	0D11	0A3
92	I/O66	0A0	0A4
93	I/O67	0A1	0A7
94	I/O68	0A2	0A8
95	I/O69	0A3	0A9
96	I/O70	0A4	0A10
97	I/O71	0A5	0A11
98	I/O72	0A6	0A12
99	I/O73	0A7	0A13
100	GND		

20446G-018

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V_{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out





144-PIN PQFP CONNECTION DIAGRAM

Top View

144-Pin PQFP

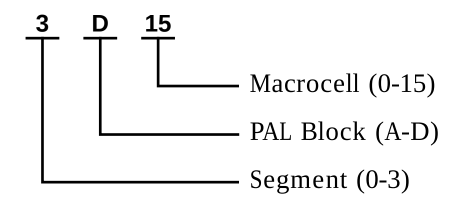
Pin	Signal	M5-128 / M5LV-128*	M5-192*	M5-256* / M5LV-256*
1	TDI			
2	I/O0	0A14	0A12	0A8
3	I/O1	0B13	0A13	0A9
4	I/O2	0B12	0A14	0A10
5	I/O3	0B11	0B13	0A11
6	I/O4	0B10	0B12	0A12
7	GND			
8	I/O5	0B8	0B11	0B13
9	I/O6	0B7	0B8	0B12
10	I/O7	0B6	0B5	0B11
11	I/O8	0B5	0B4	0B8
12	GND			
13	I/O9	0B4	0B3	0B5
14	I/O10	0B3	0B2	0B4
15	I/O11	0B2	0B1	0B3
16	I/O12	0B1	0B0	0B2
17	I0/CLK0			
18	V_{CC}			
19	GND			
20	I1/CLK1			
21	I/O13	1B1	1B0	1B2
22	I/O14	1B2	1B1	1B3
23	I/O15	1B3	1B2	1B4
24	I/O16	1B4	1B3	1B5
25	GND			
26	I/O17	1B5	1B4	1B8
27	I/O18	1B6	1B5	1B11
28	I/O19	1B7	1B8	1B12
29	I/O20	1B8	1B11	1B13
30	GND			
31	I/O21	1B10	1B12	1A12
32	I/O22	1B11	1B13	1A11
33	I/O23	1B12	1A14	1A10
34	I/O24	1B13	1A13	1A9
35	I/O25	1A14	1A12	1A8
36	TCK			
37	GND			
38	V_{CC}			
39	I/O26	1A13	1A11	1A7
40	I/O27	1A12	1A10	1A6
41	I/O28	1A11	1A8	1A5
42	I/O29	1A10	1A7	1A4
43	I/O30	1A8	1A6	1A3
44	I/O31	1A7	1A5	1A2
45	I/O32	1A6	1A4	1A1
46	GND			
47	I/O33	1A5	1A3	1D3
48	I/O34	1A4	1A2	1D4
49	I/O35	1A3	1D2	1D7
50	I/O36	1A2	1D3	1D8
51	I/O37	1A1	1D4	1D11
52	I/O38	1A0	1D7	1D12
53	V_{CC}			
54	GND			
55	GND			
56	V_{CC}			
57	I/O39	1D0	1D8	2D12
58	I/O40	1D1	1D11	2D11
59	I/O41	1D2	1D12	2D8
60	I/O42	1D3	1D13	2D7
61	I/O43	1D4	2D2	2D4
62	I/O44	1D5	2D3	2D3
63	GND			
64	I/O45	1D6	2D4	2A1
65	I/O46	1D7	2D5	2A2
66	I/O47	1D8	2D6	2A3
67	I/O48	1D10	2D7	2A4
68	I/O49	1D11	2D8	2A5
69	I/O50	1D12	2D10	2A6
70	I/O51	1D13	2D11	2A7
71	V_{CC}			
72	GND			
73	TMS			
74	I/O52	1D14	2D12	2A8
75	I/O53	1C13	2D13	2A9
76	I/O54	1C12	2D14	2A10
77	I/O55	1C11	2C13	2A11
78	I/O56	1C10	2C12	2A12
79	GND			
80	I/O57	1C8	2C11	2B13
81	I/O58	1C7	2C8	2B12
82	I/O59	1C6	2C5	2B11
83	I/O60	1C5	2C4	2B8
84	GND			
85	I/O61	1C4	2C3	2B5
86	I/O62	1C3	2C2	2B4
87	I/O63	1C2	2C1	2B3
88	I/O64	1C1	2C0	2B2
89	I2/CLK2			
90	V_{CC}			
91	GND			
92	I3/CLK3			
93	I/O65	0C1	2B0	3B2
94	I/O66	0C2	2B1	3B3
95	I/O67	0C3	2B2	3B4
96	I/O68	0C4	2B3	3B5
97	GND			
98	I/O69	0C5	2B4	3B8
99	I/O70	0C6	2B5	3B11
100	I/O71	0C7	2B8	3B12
101	I/O72	0C8	2B11	3B13
102	GND			
103	I/O73	0C10	2B12	3A12
104	I/O74	0C11	2B13	3A11
105	I/O75	0C12	2A14	3A10
106	I/O76	0C13	2A13	3A9
107	I/O77	0D14	2A12	3A8
108	TDO			
109	GND			
110	V_{CC}			
111	I/O78	0D13	2A11	3A7
112	I/O79	0D12	2A10	3A6
113	I/O80	0D11	2A8	3A5
114	I/O81	0D10	2A7	3A4
115	I/O82	0D8	2A6	3A3
116	I/O83	0D7	2A5	3A2
117	I/O84	0D6	2A4	3A1
118	GND			
119	I/O85	0D5	2A3	3D3
120	I/O86	0D4	2A2	3D4
121	I/O87	0D3	0D13	3D7
122	I/O88	0D2	0D12	3D8
123	I/O89	0D1	0D11	3D11
124	I/O90	0D0	0D8	3D12
125	V_{CC}			
126	GND			
127	GND			
128	V_{CC}			
129	I/O91	0A0	0D7	0D12
130	I/O92	0A1	0D4	0D11
131	I/O93	0A2	0D3	0D8
132	I/O94	0A3	0D2	0D7
133	I/O95	0A4	0A2	0D4
134	I/O96	0A5	0A3	0D3
135	GND			
136	I/O97	0A6	0A4	0A1
137	I/O98	0A7	0A5	0A2
138	I/O99	0A8	0A6	0A3
139	I/O100	A10	0A7	0A4
140	I/O101	0A11	0A8	0A5
141	I/O102	0A12	0A10	0A6
142	I/O103	0A13	0A11	0A7
143	V_{CC}			
144	GND			

*Package obsolete, contact factory.

20446G-019

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V_{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out





144-PIN TQFP CONNECTION DIAGRAM

Top View

144-Pin TQFP

Left side (pins 1–36)

M5LV-128	M5LV-256	Signal	Pin
		TDI	1
0A14	0A8	I/O0	2
0B13	0A9	I/O1	3
0B12	0A10	I/O2	4
0B11	0A11	I/O3	5
0B10	0A12	I/O4	6
		GND	7
0B8	0B13	I/O5	8
0B7	0B12	I/O6	9
0B6	0B11	I/O7	10
0B5	0B8	I/O8	11
		GND	12
0B4	0B5	I/O9	13
0B3	0B4	I/O10	14
0B2	0B3	I/O11	15
0B1	0B2	I/O12	16
		I0/CLK0	17
		V_{CC}	18
		GND	19
		I1/CLK1	20
1B1	1B2	I/O13	21
1B2	1B3	I/O14	22
1B3	1B4	I/O15	23
1B4	1B5	I/O16	24
		GND	25
1B5	1B8	I/O17	26
1B6	1B11	I/O18	27
1B7	1B12	I/O19	28
1B8	1B13	I/O20	29
		GND	30
1B10	1A12	I/O21	31
1B11	1A11	I/O22	32
1B12	1A10	I/O23	33
1B13	1A9	I/O24	34
1A14	1A8	I/O25	35
		TCK	36

Bottom side (pins 37–72)

Pin	Signal	M5LV-256	M5LV-128
37	GND		
38	V_{CC}		
39	I/O26	1A7	1A13
40	I/O27	1A6	1A12
41	I/O28	1A5	1A11
42	I/O29	1A4	1A10
43	I/O30	1A3	1A8
44	I/O31	1A2	1A7
45	I/O32	1A1	1A6
46	GND		
47	I/O33	1D3	1A5
48	I/O34	1D4	1A4
49	I/O35	1D7	1A3
50	I/O36	1D8	1A2
51	I/O37	1D11	1A1
52	I/O38	1D12	1A0
53	V_{CC}		
54	GND		
55	GND		
56	V_{CC}		
57	I/O39	2D12	1D0
58	I/O40	2D11	1D1
59	I/O41	2D8	1D2
60	I/O42	2D7	1D3
61	I/O43	2D4	1D4
62	I/O44	2D3	1D5
63	GND		
64	I/O45	2A1	1D6
65	I/O46	2A2	1D7
66	I/O47	2A3	1D8
67	I/O48	2A4	1D10
68	I/O49	2A5	1D11
69	I/O50	2A6	1D12
70	I/O51	2A7	1D13
71	V_{CC}		
72	GND		

Right side (pins 73–108)

Pin	Signal	M5LV-256	M5LV-128
108	TDO		
107	I/O77	3A8	0D14
106	I/O76	3A9	0C13
105	I/O75	3A10	0C12
104	I/O74	3A11	0C11
103	I/O73	3A12	0C10
102	GND		
101	I/O72	3B13	0C8
100	I/O71	3B12	0C7
99	I/O70	3B11	0C6
98	I/O69	3B8	0C5
97	GND		
96	I/O68	3B5	0C4
95	I/O67	3B4	0C3
94	I/O66	3B3	0C2
93	I/O65	3B2	0C1
92	I3/CLK3		
91	GND		
90	V_{CC}		
89	I2/CLK2		
88	I/O64	2B2	1C1
87	I/O63	2B3	1C2
86	I/O62	2B4	1C3
85	I/O61	2B5	1C4
84	GND		
83	I/O60	2B8	1C5
82	I/O59	2B11	1C6
81	I/O58	2B12	1C7
80	I/O57	2B13	1C8
79	GND		
78	I/O56	2A12	1C10
77	I/O55	2A11	1C11
76	I/O54	2A10	1C12
75	I/O53	2A9	1C13
74	I/O52	2A8	1D14
73	TMS		

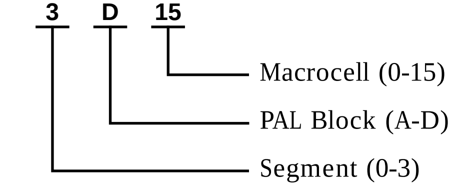
Top side (pins 109–144)

Pin	Signal	M5LV-256	M5LV-128
144	GND		
143	V_{CC}		
142	I/O103	0A7	0A13
141	I/O102	0A6	0A12
140	I/O101	0A5	0A11
139	I/O100	0A4	A10
138	I/O99	0A3	0A8
137	I/O98	0A2	0A7
136	I/O97	0A1	0A6
135	GND		
134	I/O96	0D3	0A5
133	I/O95	0D4	0A4
132	I/O94	0D7	0A3
131	I/O93	0D8	0A2
130	I/O92	0D11	0A1
129	I/O91	0D12	0A0
128	V_{CC}		
127	GND		
126	GND		
125	V_{CC}		
124	I/O90	3D12	0D0
123	I/O89	3D11	0D1
122	I/O88	3D8	0D2
121	I/O87	3D7	0D3
120	I/O86	3D4	0D4
119	I/O85	3D3	0D5
118	GND		
117	I/O84	3A1	0D6
116	I/O83	3A2	0D7
115	I/O82	3A3	0D8
114	I/O81	3A4	0D10
113	I/O80	3A5	0D11
112	I/O79	3A6	0D12
111	I/O78	3A7	0D13
110	V_{CC}		
109	GND		

20446G-020

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V_{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out





160-PIN PQFP CONNECTION DIAGRAM

Top View

160-Pin PQFP (128, 192, 256 Macrocells)

Top side (pins 160–121):

Pin	Signal	M5-128 / M5LV-128	M5-192	M5-256 / M5LV-256
160	GND			
159	V_{CC}			
158	I/O119	0A13	0A11	0A7
157	I/O118	0A12	0A10	0A6
156	I/O117	0A11	0A9	0A5
155	I/O116	0A10	0A8	0A4
154	I/O115	0A9	0A7	0A3
153	I/O114	0A8	0A6	0A2
152	I/O113	0A7	0A5	0A1
151	I/O112	0A6	0A4	0A0
150	GND			
149	V_{CC}			
148	I/O111	0A5	0A3	0D3
147	I/O110	0A4	0A2	0D4
146	I/O109	0A3	0D2	0D7
145	I/O108	0A2	0D3	0D8
144	I/O107	0A1	0D4	0D11
143	I/O106	0A0	0D7	0D12
142	V_{CC}			
141	GND			
140	GND			
139	V_{CC}			
138	I/O105	0D0	0D8	3D12
137	I/O104	0D1	0D11	3D11
136	I/O103	0D2	0D12	3D8
135	I/O102	0D3	0D13	3D7
134	I/O101	0D4	2A2	3D4
133	I/O100	0D5	2A3	3D3
132	V_{CC}			
131	GND			
130	I/O99	0D6	2A4	3A0
129	I/O98	0D7	2A5	3A1
128	I/O97	0D8	2A6	3A2
127	I/O96	0D9	2A7	3A3
126	I/O95	0D10	2A8	3A4
125	I/O94	0D11	2A9	3A5
124	I/O93	0D12	2A10	3A6
123	I/O92	0D13	2A11	3A7
122	V_{CC}			
121	GND			

Left side (pins 1–40):

Pin	Signal	M5-128 / M5LV-128	M5-192	M5-256 / M5LV-256
1	TDI			
2	I/O0	0A14	0A12	0A8
3	I/O1	0A15	0A13	0A9
4	I/O2	0B14	0A14	0A10
5	I/O3	0B13	0A15	0A11
6	I/O4	0B12	0B15	0A12
7	I/O5	0B11	0B14	0A13
8	I/O6	0B10	0B13	0A14
9	I/O7	0B9	0B12	0A15
10	GND			
11	I/O8	0B8	0B11	0B13
12	I/O9	0B7	0B8	0B12
13	I/O10	0B6	0B5	0B11
14	I/O11	0B5	0B4	0B8
15	I/O12	0B4	0B3	0B5
16	I/O13	0B3	0B2	0B4
17	I/O14	0B2	0B1	0B3
18	I/O15	0B1	0B0	0B2
19	I0/CLK0			
20	V_{CC}			
21	GND			
22	I1/CLK1			
23	I/O16	1B1	1B0	1B2
24	I/O17	1B2	1B1	1B3
25	I/O18	1B3	1B2	1B4
26	I/O19	1B4	1B3	1B5
27	I/O20	1B5	1B4	1B8
28	I/O21	1B6	1B5	1B11
29	I/O22	1B7	1B8	1B12
30	I/O23	1B8	1B11	1B13
31	GND			
32	I/O24	1B9	1B12	1A15
33	I/O25	1B10	1B13	1A14
34	I/O26	1B11	1B14	1A13
35	I/O27	1B12	1B15	1A12
36	I/O28	1B13	1A15	1A11
37	I/O29	1B14	1A14	1A10
38	I/O30	1A15	1A13	1A9
39	I/O31	1A14	1A12	1A8
40	TCK			

Bottom side (pins 41–80):

Pin	Signal	M5-128 / M5LV-128	M5-192	M5-256 / M5LV-256
41	GND			
42	V_{CC}			
43	I/O32	1A13	1A11	1A7
44	I/O33	1A12	1A10	1A6
45	I/O34	1A11	1A9	1A5
46	I/O35	1A10	1A8	1A4
47	I/O36	1A9	1A7	1A3
48	I/O37	1A8	1A6	1A2
49	I/O38	1A7	1A5	1A1
50	I/O39	1A6	1A4	1A0
51	GND			
52	V_{CC}			
53	I/O40	1A5	1A3	1D3
54	I/O41	1A4	1A2	1D4
55	I/O42	1A3	1D2	1D7
56	I/O43	1A2	1D3	1D8
57	I/O44	1A1	1D4	1D11
58	I/O45	1A0	1D7	1D12
59	V_{CC}			
60	GND			
61	GND			
62	V_{CC}			
63	I/O46	1D0	1D8	2D12
64	I/O47	1D1	1D11	2D11
65	I/O48	1D2	1D12	2D8
66	I/O49	1D3	1D13	2D7
67	I/O50	1D4	2D2	2D4
68	I/O51	1D5	2D3	2D3
69	V_{CC}			
70	GND			
71	I/O52	1D6	2D4	2A0
72	I/O53	1D7	2D5	2A1
73	I/O54	1D8	2D6	2A2
74	I/O55	1D9	2D7	2A3
75	I/O56	1D10	2D8	2A4
76	I/O57	1D11	2D9	2A5
77	I/O58	1D12	2D10	2A6
78	I/O59	1D13	2D11	2A7
79	V_{CC}			
80	GND			

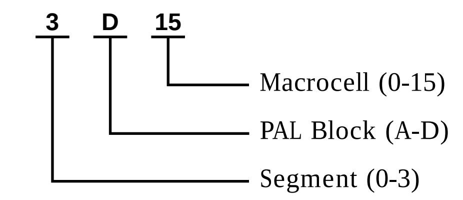
Right side (pins 120–81):

Pin	Signal	M5-128 / M5LV-128	M5-192	M5-256 / M5LV-256
120	TDO			
119	I/O91	0D14	2A12	3A8
118	I/O90	0D15	2A13	3A9
117	I/O89	0C14	2A14	3A10
116	I/O88	0C13	2A15	3A11
115	I/O87	0C12	2B15	3A12
114	I/O86	0C11	2B14	3A13
113	I/O85	0C10	2B13	3A14
112	I/O84	0C9	2B12	3A15
111	GND			
110	I/O83	0C8	2B11	3B13
109	I/O82	0C7	2B8	3B12
108	I/O81	0C6	2B5	3B11
107	I/O80	0C5	2B4	3B8
106	I/O79	0C4	2B3	3B5
105	I/O78	0C3	2B2	3B4
104	I/O77	0C2	2B1	3B3
103	I/O76	0C1	2B0	3B2
102	I3/CLK3			
101	GND			
100	V_{CC}			
99	I2/CLK2			
98	I/O75	1C1	2C0	2B2
97	I/O74	1C2	2C1	2B3
96	I/O73	1C3	2C2	2B4
95	I/O72	1C4	2C3	2B5
94	I/O71	1C5	2C4	2B8
93	I/O70	1C6	2C5	2B11
92	I/O69	1C7	2C8	2B12
91	I/O68	1C8	2C11	2B13
90	GND			
89	I/O67	1C9	2C12	2A15
88	I/O66	1C10	2C13	2A14
87	I/O65	1C11	2C14	2A13
86	I/O64	1C12	2C15	2A12
85	I/O63	1C13	2D15	2A11
84	I/O62	1C14	2D14	2A10
83	I/O61	1D15	2D13	2A9
82	I/O60	1D14	2D12	2A8
81	TMS			

20446G-021

Pin Designations

CLK	=	Clock	V_{CC}	=	Supply Voltage
GND	=	Ground	TDI	=	Test Data In
I	=	Input	TCK	=	Test Clock
I/O	=	Input/Output	TMS	=	Test Mode Select
NC	=	No Connect	TDO	=	Test Data Out





160-PIN PQFP (WITH INTERNAL HEAT SPREADER) CONNECTION DIAGRAM

Top View

160-Pin PQFP (320, 384, 512 Macrocells)

Left side (pins 1–40)

Pin	Signal	M5-512*/M5LV-512	M5-384*/M5LV-384	M5-320*/M5LV-320
1	TDI			
2	I/O0	0A2	0A2	0A2
3	I/O1	0A3	0A3	0A3
4	I/O2	0A4	0A4	0A4
5	I/O3	0A7	0A7	0A7
6	I/O4	0A8	0A8	0A8
7	I/O5	0A11	0A11	0A11
8	I/O6	0A12	0A12	0A12
9	I/O7	0A13	0A13	0A13
10	GND			
11	I/O8	0D13	0D13	0D13
12	I/O9	0D12	0D12	0D12
13	I/O10	0D11	0D11	0D11
14	I/O11	0D8	0D8	0D8
15	I/O12	0D7	0D7	0D7
16	I/O13	0D4	0D4	0D4
17	I/O14	0D3	0D3	0D3
18	I/O15	0D2	0D2	0D2
19	I0/CLK0			
20	V_{CC}			
21	GND			
22	I1/CLK1			
23	I/O16	1D2	1D2	1D2
24	I/O17	1D3	1D3	1D3
25	I/O18	1D4	1D4	1D4
26	I/O19	1D7	1D7	1D7
27	I/O20	1D8	1D8	1D8
28	I/O21	1D11	1D11	1D11
29	I/O22	1D12	1D12	1D12
30	I/O23	1D13	1D13	1D13
31	GND			
32	I/O24	1A13	1A13	1A15
33	I/O25	1A12	1A12	1A14
34	I/O26	1A11	1A11	1A13
35	I/O27	1A8	1A8	1A12
36	I/O28	1A7	1A7	1A11
37	I/O29	1A4	1A4	1A10
38	I/O30	1A3	1A3	1A9
39	I/O31	1A2	1A2	1A8
40	TCK			

Bottom side (pins 41–80)

Pin	Signal	M5-512*/M5LV-512	M5-384*/M5LV-384	M5-320*/M5LV-320
41	GND			
42	V_{CC}			
43	I/O32	2A13	1B2	1A7
44	I/O33	2A12	1B3	1A6
45	I/O34	2A11	1B4	1A5
46	I/O35	2A8	1B7	1A4
47	I/O36	2A7	1B8	1A3
48	I/O37	2A4	1B11	1A2
49	I/O38	2A3	1B12	1A1
50	I/O39	2A2	1B13	1A0
51	GND			
52	V_{CC}			
53	I/O40	2B3	2A12	1B3
54	I/O41	2B4	2A11	1B4
55	I/O42	2B7	2A8	1B7
56	I/O43	2B8	2A7	1B8
57	I/O44	2B11	2A4	1B11
58	I/O45	2B12	2A3	1B12
59	V_{CC}			
60	GND			
61	GND			
62	V_{CC}			
63	I/O46	3B12	2B3	2B12
64	I/O47	3B11	2B4	2B11
65	I/O48	3B8	2B7	2B8
66	I/O49	3B7	2B8	2B7
67	I/O50	3B4	2B11	2B4
68	I/O51	3B3	2B12	2B3
69	V_{CC}			
70	GND			
71	I/O52	3A2	3B13	2A0
72	I/O53	3A3	3B12	2A1
73	I/O54	3A4	3B11	2A2
74	I/O55	3A7	3B8	2A3
75	I/O56	3A8	3B7	2A4
76	I/O57	3A11	3B4	2A5
77	I/O58	3A12	3B3	2A6
78	I/O59	3A13	3B2	2A7
79	V_{CC}			
80	GND			

Right side (pins 81–120)

Pin	Signal	M5-512*/M5LV-512	M5-384*/M5LV-384	M5-320*/M5LV-320
120	TDO			
119	I/O91	5A2	4A2	3A2
118	I/O90	5A3	4A3	3A3
117	I/O89	5A4	4A4	3A4
116	I/O88	5A7	4A7	3A7
115	I/O87	5A8	4A8	3A8
114	I/O86	5A11	4A11	3A11
113	I/O85	5A12	4A12	3A12
112	I/O84	5A13	4A13	3A13
111	GND			
110	I/O83	5D13	4D13	3D13
109	I/O82	5D12	4D12	3D12
108	I/O81	5D11	4D11	3D11
107	I/O80	5D8	4D8	3D8
106	I/O79	5D7	4D7	3D7
105	I/O78	5D4	4D4	3D4
104	I/O77	5D3	4D3	3D3
103	I/O76	5D2	4D2	3D2
102	I3/CLK3			
101	GND			
100	V_{CC}			
99	I2/CLK2			
98	I/O75	4D2	3D2	2D2
97	I/O74	4D3	3D3	2D3
96	I/O73	4D4	3D4	2D4
95	I/O72	4D7	3D7	2D7
94	I/O71	4D8	3D8	2D8
93	I/O70	4D11	3D11	2D11
92	I/O69	4D12	3D12	2D12
91	I/O68	4D13	3D13	2D13
90	GND			
89	I/O67	4A13	3A13	2A15
88	I/O66	4A12	3A12	2A14
87	I/O65	4A11	3A11	2A13
86	I/O64	4A8	3A8	2A12
85	I/O63	4A7	3A7	2A11
84	I/O62	4A4	3A4	2A10
83	I/O61	4A3	3A3	2A9
82	I/O60	4A2	3A2	2A8
81	TMS			

Top side (pins 121–160)

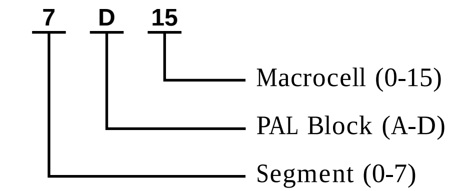
Pin	Signal	M5-512*/M5LV-512	M5-384*/M5LV-384	M5-320*/M5LV-320
160	GND			
159	V_{CC}			
158	I/O119	7A13	0B2	0B2
157	I/O118	7A12	0B3	0B3
156	I/O117	7A11	0B4	0B4
155	I/O116	7A8	0B7	0B7
154	I/O115	7A7	0B8	0B8
153	I/O114	7A4	0B11	0B11
152	I/O113	7A3	0B12	0B12
151	I/O112	7A2	0B13	0B13
150	GND			
149	V_{CC}			
148	I/O111	7B3	5A12	4A12
147	I/O110	7B4	5A11	4A11
146	I/O109	7B7	5A8	4A8
145	I/O108	7B8	5A7	4A7
144	I/O107	7B11	5A4	4A4
143	I/O106	7B12	5A3	4A3
142	V_{CC}			
141	GND			
140	GND			
139	V_{CC}			
138	I/O105	6B12	5B3	4B3
137	I/O104	6B11	5B4	4B4
136	I/O103	6B8	5B7	4B7
135	I/O102	6B7	5B8	4B8
134	I/O101	6B4	5B11	4B11
133	I/O100	6B3	5B12	4B12
132	V_{CC}			
131	GND			
130	I/O99	6A2	4B13	3B13
129	I/O98	6A3	4B12	3B12
128	I/O97	6A4	4B11	3B11
127	I/O96	6A7	4B8	3B8
126	I/O95	6A8	4B7	3B7
125	I/O94	6A11	4B4	3B4
124	I/O93	6A12	4B3	3B3
123	I/O92	6A13	4B2	3B2
122	V_{CC}			
121	GND			

*Package obsolete, contact factory.

20446G-022

Pin Designations

CLK	= Clock	V_{CC}	= Supply Voltage		
GND	= Ground	TDI	= Test Data In		
I	= Input	TCK	= Test Clock		
I/O	= Input/Output	TMS	= Test Mode Select		
NC	= No Connect	TDO	= Test Data Out		



208-PIN PQFP CONNECTION DIAGRAM

Top View

208-Pin PQFP (192, 256 Macrocells)

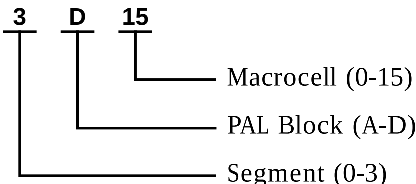
M5-256
M5LV-256

Pin	Signal	Macrocell
1	TDI	
2	I/O0	0A8
3	I/O1	0A9
4	I/O2	0A10
5	I/O3	0A11
6	I/O4	0A12
7	I/O5	0A13
8	I/O6	0A14
9	I/O7	0A15
10	V_{CC}	
11	GND	
12	I/O8	0B13
13	I/O9	0B12
14	I/O10	0B11
15	I/O11	0B10
16	I/O12	0B9
17	I/O13	0B8
18	I/O14	0B7
19	I/O15	0B6
20	GND	
21	I/O16	0B5
22	I/O17	0B4
23	I/O18	0B3
24	I/O19	0B2
25	I0/CLK0	
26	V_{CC}	
27	GND	
28	I1/CLK1	
29	I/O20	1B2
30	I/O21	1B3
31	I/O22	1B4
32	I/O23	1B5
33	GND	
34	I/O24	1B6
35	I/O25	1B7
36	I/O26	1B8
37	I/O27	1B9
38	I/O28	1B10
39	I/O29	1B11
40	I/O30	1B12
41	I/O31	1B13
42	GND	
43	V_{CC}	
44	I/O32	1A15
45	I/O33	1A14
46	I/O34	1A13
47	I/O35	1A12
48	I/O36	1A11
49	I/O37	1A10
50	I/O38	1A9
51	I/O39	1A8
52	TCK	
53	GND	
54	I/O40	1A7
55	I/O41	1A6
56	I/O42	1A5
57	I/O43	1A4
58	I/O44	1A3
59	I/O45	1A2
60	I/O46	1A1
61	I/O47	1A0
62	GND	
63	V_{CC}	
64	I/O48	1D2
65	I/O49	1D3
66	I/O50	1D4
67	I/O51	1D5
68	I/O52	1D6
69	I/O53	1D7
70	I/O54	1D8
71	I/O55	1D9
72	GND	
73	I/O56	1D10
74	I/O57	1D11
75	I/O58	1D12
76	I/O59	1D13
77	V_{CC}	
78	GND	
79	GND	
80	V_{CC}	
81	I/O60	2D13
82	I/O61	2D12
83	I/O62	2D11
84	I/O63	2D10
85	GND	
86	I/O64	2D9
87	I/O65	2D8
88	I/O66	2D7
89	I/O67	2D6
90	I/O68	2D5
91	I/O69	2D4
92	I/O70	2D3
93	I/O71	2D2
94	V_{CC}	
95	GND	
96	I/O72	2A0
97	I/O73	2A1
98	I/O74	2A2
99	I/O75	2A3
100	I/O76	2A4
101	I/O77	2A5
102	I/O78	2A6
103	I/O79	2A7
104	GND	
105	TMS	
106	I/O80	2A8
107	I/O81	2A9
108	I/O82	2A10
109	I/O83	2A11
110	I/O84	2A12
111	I/O85	2A13
112	I/O86	2A14
113	I/O87	2A15
114	V_{CC}	
115	GND	
116	I/O88	2B13
117	I/O89	2B12
118	I/O90	2B11
119	I/O91	2B10
120	I/O92	2B9
121	I/O93	2B8
122	I/O94	2B7
123	I/O95	2B6
124	GND	
125	I/O96	2B5
126	I/O97	2B4
127	I/O98	2B3
128	I/O99	2B2
129	I2/CLK2	
130	V_{CC}	
131	GND	
132	I3/CLK3	
133	I/O100	3B2
134	I/O101	3B3
135	I/O102	3B4
136	I/O103	3B5
137	GND	
138	I/O104	3B6
139	I/O105	3B7
140	I/O106	3B8
141	I/O107	3B9
142	I/O108	3B10
143	I/O109	3B11
144	I/O110	3B12
145	I/O111	3B13
146	GND	
147	V_{CC}	
148	I/O112	3A15
149	I/O113	3A14
150	I/O114	3A13
151	I/O115	2A12
152	I/O116	3A11
153	I/O117	3A10
154	I/O118	3A9
155	I/O119	3A8
156	TDO	
157	GND	
158	I/O120	3A7
159	I/O121	3A6
160	I/O122	3A5
161	I/O123	3A4
162	I/O124	3A3
163	I/O125	3A2
164	I/O126	3A1
165	I/O127	3A0
166	GND	
167	V_{CC}	
168	I/O128	3D2
169	I/O129	3D3
170	I/O130	3D4
171	I/O131	3D5
172	I/O132	3D6
173	I/O133	3D7
174	I/O134	3D8
175	I/O135	3D9
176	GND	
177	I/O136	3D10
178	I/O137	3D11
179	I/O138	3D12
180	I/O139	3D13
181	V_{CC}	
182	GND	
183	GND	
184	V_{CC}	
185	I/O140	0D13
186	I/O141	0D12
187	I/O142	0D11
188	I/O143	0D10
189	GND	
190	I/O144	0D9
191	I/O145	0D8
192	I/O146	0D7
193	I/O147	0D6
194	I/O148	0D5
195	I/O149	0D4
196	I/O150	0D3
197	I/O151	0D2
198	V_{CC}	
199	GND	
200	I/O152	0A0
201	I/O153	0A1
202	I/O154	0A2
203	I/O155	0A3
204	I/O156	0A4
205	I/O157	0A5
206	I/O158	0A6
207	I/O159	0A7
208	GND	

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Pin Designations

CLK	= Clock	V_{CC}	= Supply Voltage
GND	= Ground	TDI	= Test Data In
I	= Input	TCK	= Test Clock
I/O	= Input/Output	TMS	= Test Mode Select
NC	= No Connect	TDO	= Test Data Out





208-PIN PQFP (WITH INTERNAL HEAT SPREADER) CONNECTION DIAGRAM

Top View

208-Pin PQFP (320, 384, 512 Macrocells)

Left side (pins 1–52)

M5-320 / M5LV-320	M5-384 / M5LV-384	M5-512 / M5LV-512	Signal	Pin
			TDI	1
0A2	0A2	0A2	I/O0	2
0A3	0A3	0A3	I/O1	3
0A4	0A4	0A4	I/O2	4
0A7	0A7	0A7	I/O3	5
0A8	0A8	0A8	I/O4	6
0A11	0A11	0A11	I/O5	7
0A12	0A12	0A12	I/O6	8
0A13	0A13	0A13	I/O7	9
			V_{CC}	10
			GND	11
0D15	0D15	0D15	I/O8	12
0D14	0D14	0D14	I/O9	13
0D13	0D13	0D13	I/O10	14
0D12	0D12	0D12	I/O11	15
0D11	0D11	0D11	I/O12	16
0D10	0D10	0D10	I/O13	17
0D9	0D9	0D9	I/O14	18
0D8	0D8	0D8	I/O15	19
			GND	20
0D7	0D7	0D7	I/O16	21
0D4	0D4	0D4	I/O17	22
0D3	0D3	0D3	I/O18	23
0D2	0D2	0D2	I/O19	24
			I0/CLK0	25
			V_{CC}	26
			GND	27
			I1/CLK1	28
1D2	1D2	1D2	I/O20	29
1D3	1D3	1D3	I/O21	30
1D4	1D4	1D4	I/O22	31
1D7	1D7	1D7	I/O23	32
			GND	33
1D8	1D8	1D8	I/O24	34
1D9	1D9	1D9	I/O25	35
1D10	1D10	1D10	I/O26	36
1D11	1D11	1D11	I/O27	37
1D12	1D12	1D12	I/O28	38
1D13	1D13	1D13	I/O29	39
1D14	1D14	1D14	I/O30	40
1D15	1D15	1D15	I/O31	41
			GND	42
			V_{CC}	43
1A15	1A13	1A13	I/O32	44
1A14	1A12	1A12	I/O33	45
1A13	1A11	1A11	I/O34	46
1A12	1A8	1A8	I/O35	47
1A11	1A7	1A7	I/O36	48
1A10	1A4	1A4	I/O37	49
1A9	1A3	1A3	I/O38	50
1A8	1A2	1A2	I/O39	51
			TCK	52

Bottom side (pins 53–104)

Pin	Signal	M5-512 / M5LV-512	M5-384 / M5LV-384	M5-320 / M5LV-320
53	GND			
54	I/O40	2A13	1B2	1A7
55	I/O41	2A12	1B3	1A6
56	I/O42	2A11	1B4	1A5
57	I/O43	2A8	1B7	1A4
58	I/O44	2A7	1B8	1A3
59	I/O45	2A4	1B11	1A2
60	I/O46	2A3	1B12	1A1
61	I/O47	2A2	1B13	1A0
62	GND			
63	V_{CC}			
64	I/O48	2B0	2A15	1B0
65	I/O49	2B1	2A14	1B1
66	I/O50	2B2	2A13	1B2
67	I/O51	2B3	2A12	1B3
68	I/O52	2B4	2A11	1B4
69	I/O53	2B5	2A10	1B5
70	I/O54	2B6	2A9	1B6
71	I/O55	2B7	2A8	1B7
72	GND			
73	I/O56	2B8	2A7	1B8
74	I/O57	2B11	2A4	1B11
75	I/O58	2B12	2A3	1B12
76	I/O59	2B13	2A2	1B13
77	V_{CC}			
78	GND			
79	GND			
80	V_{CC}			
81	I/O60	3B13	2B2	2B13
82	I/O61	3B12	2B3	2B12
83	I/O62	3B11	2B4	2B11
84	I/O63	3B8	2B7	2B8
85	GND			
86	I/O64	3B7	2B8	2B7
87	I/O65	3B6	2B9	2B6
88	I/O66	3B5	2B10	2B5
89	I/O67	3B4	2B11	2B4
90	I/O68	3B3	2B12	2B3
91	I/O69	3B2	2B13	2B2
92	I/O70	3B1	2B14	2B1
93	I/O71	3B0	2B15	2B0
94	V_{CC}			
95	GND			
96	I/O72	3A2	3B13	2A0
97	I/O73	3A3	3B12	2A1
98	I/O74	3A4	3B11	2A2
99	I/O75	3A7	3B8	2A3
100	I/O76	3A8	3B7	2A4
101	I/O77	3A11	3B4	2A5
102	I/O78	3A12	3B3	2A6
103	I/O79	3A13	3B2	2A7
104	GND			

Right side (pins 105–156)

Pin	Signal	M5-512 / M5LV-512	M5-384 / M5LV-384	M5-320 / M5LV-320
156	TDO			
155	I/O119	5A2	4A2	3A2
154	I/O118	5A3	4A3	3A3
153	I/O117	5A4	4A4	3A4
152	I/O116	5A7	4A7	3A7
151	I/O115	5A8	4A8	3A8
150	I/O114	5A11	4A11	3A11
149	I/O113	5A12	4A12	3A12
148	I/O112	5A13	4A13	3A13
147	V_{CC}			
146	GND			
145	I/O111	5D15	4D15	3D15
144	I/O110	5D14	4D14	3D14
143	I/O109	5D13	4D13	3D13
142	I/O108	5D12	4D12	3D12
141	I/O107	5D11	4D11	3D11
140	I/O106	5D10	4D10	3D10
139	I/O105	5D9	4D9	3D9
138	I/O104	5D8	4D8	3D8
137	GND			
136	I/O103	5D7	4D7	3D7
135	I/O102	5D4	4D4	3D4
134	I/O101	5D3	4D3	3D3
133	I/O100	5D2	4D2	3D2
132	I3/CLK3			
131	GND			
130	V_{CC}			
129	I2/CLK2			
128	I/O99	4D2	3D2	2D2
127	I/O98	4D3	3D3	2D3
126	I/O97	4D4	3D4	2D4
125	I/O96	4D7	3D7	2D7
124	GND			
123	I/O95	4D8	3D8	2D8
122	I/O94	4D9	3D9	2D9
121	I/O93	4D10	3D10	2D10
120	I/O92	4D11	3D11	2D11
119	I/O91	4D12	3D12	2D12
118	I/O90	4D13	3D13	2D13
117	I/O89	4D14	3D14	2D14
116	I/O88	4D15	3D15	2D15
115	GND			
114	V_{CC}			
113	I/O87	4A13	3A13	2A15
112	I/O86	4A12	3A12	2A14
111	I/O85	4A11	3A11	2A13
110	I/O84	4A8	3A8	2A12
109	I/O83	4A7	3A7	2A11
108	I/O82	4A4	3A4	2A10
107	I/O81	4A3	3A3	2A9
106	I/O80	4A2	3A2	2A8
105	TMS			

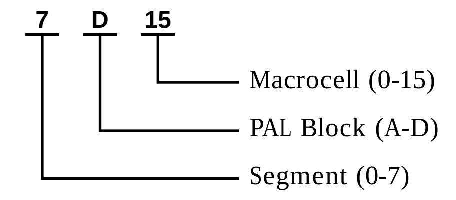
Top side (pins 157–208)

Pin	Signal	M5-512 / M5LV-512	M5-384 / M5LV-384	M5-320 / M5LV-320
208	GND			
207	I/O159	7A13	0B2	0B2
206	I/O158	7A12	0B3	0B3
205	I/O157	7A11	0B4	0B4
204	I/O156	7A8	0B7	0B7
203	I/O155	7A7	0B8	0B8
202	I/O154	7A4	0B11	0B11
201	I/O153	7A3	0B12	0B12
200	I/O152	7A2	0B13	0B13
199	GND			
198	V_{CC}			
197	I/O151	7B0	5A15	4A15
196	I/O150	7B1	5A14	4A14
195	I/O149	7B2	5A13	4A13
194	I/O148	7B3	5A12	4A12
193	I/O147	7B4	5A11	4A11
192	I/O146	7B5	5A10	4A10
191	I/O145	7B6	5A9	4A9
190	I/O144	7B7	5A8	4A8
189	GND			
188	I/O143	7B8	5A7	4A7
187	I/O142	7B11	5A4	4A4
186	I/O141	7B12	5A3	4A3
185	I/O140	7B13	5A2	4A2
184	V_{CC}			
183	GND			
182	GND			
181	V_{CC}			
180	I/O139	6B13	5B2	4B2
179	I/O138	6B12	5B3	4B3
178	I/O137	6B11	5B4	4B4
177	I/O136	6B8	5B7	4B7
176	GND			
175	I/O135	6B7	5B8	4B8
174	I/O134	6B6	5B9	4B9
173	I/O133	6B5	5B10	4B10
172	I/O132	6B4	5B11	4B11
171	I/O131	6B3	5B12	4B12
170	I/O130	6B2	5B13	4B13
169	I/O129	6B1	5B14	4B14
168	I/O128	6B0	5B15	4B15
167	V_{CC}			
166	GND			
165	I/O127	6A2	4B13	3B13
164	I/O126	6A3	4B12	3B12
163	I/O125	6A4	4B11	3B11
162	I/O124	6A7	4B8	3B8
161	I/O123	6A8	4B7	3B7
160	I/O122	6A11	4B4	3B4
159	I/O121	6A12	4B3	3B3
158	I/O120	6A13	4B2	3B2
157	GND			

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Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V_{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out





240-PIN PQFP CONNECTION DIAGRAM

Top View

240-Pin PQFP

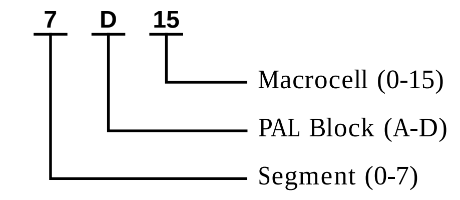
Pin	Signal	M5-512* / M5LV-512*	M5-384* / M5LV-384*	M5-320* / M5LV-320*
1	TDI			
2	I/O0	0A2	0A2	0A2
3	I/O1	0A3	0A3	0A3
4	I/O2	0A4	0A4	0A4
5	I/O3	0A7	0A7	0A7
6	I/O4	0A8	0A8	0A8
7	I/O5	0A11	0A11	0A11
8	I/O6	0A12	0A12	0A12
9	I/O7	0A13	0A13	0A13
10	V_{CC}			
11	GND			
12	I/O8	0D15	0D15	0D15
13	I/O9	0D14	0D14	0D14
14	I/O10	0D13	0D13	0D13
15	I/O11	0D12	0D12	0D12
16	I/O12	0D11	0D11	0D11
17	I/O13	0D10	0D10	0D10
18	I/O14	0D9	0D9	0D9
19	I/O15	0D8	0D8	0D8
20	GND			
21	I/O16	0D7	0D7	0D7
22	I/O17	0D6	0D6	0D6
23	I/O18	0D5	0D5	0D5
24	I/O19	0D4	0D4	0D4
25	I/O20	0D3	0D3	0D3
26	I/O21	0D2	0D2	0D2
27	I/O22	0D1	0D1	0D1
28	I/O23	0D0	0D0	0D0
29	I0/CLK0			
30	V_{CC}			
31	GND			
32	I1/CLK1			
33	I/O24	1D0	1D0	1D0
34	I/O25	1D1	1D1	1D1
35	I/O26	1D2	1D2	1D2
36	I/O27	1D3	1D3	1D3
37	I/O28	1D4	1D4	1D4
38	I/O29	1D5	1D5	1D5
39	I/O30	1D6	1D6	1D6
40	I/O31	1D7	1D7	1D7
41	GND			
42	I/O32	1D8	1D8	1D8
43	I/O33	1D9	1D9	1D9
44	I/O34	1D10	1D10	1D10
45	I/O35	1D11	1D11	1D11
46	I/O36	1D12	1D12	1D12
47	I/O37	1D13	1D13	1D13
48	I/O38	1D14	1D14	1D14
49	I/O39	1D15	1D15	1D15
50	GND			
51	V_{CC}			
52	I/O40	1A13	1A13	1A15
53	I/O41	1A12	1A12	1A14
54	I/O42	1A11	1A11	1A13
55	I/O43	1A8	1A8	1A12
56	I/O44	1A7	1A7	1A11
57	I/O45	1A4	1A4	1A10
58	I/O46	1A3	1A3	1A9
59	I/O47	1A2	1A2	1A8
60	TCK			
61	GND			
62	V_{CC}			
63	I/O48	2A13	1B2	1A7
64	I/O49	2A12	1B3	1A6
65	I/O50	2A11	1B4	1A5
66	I/O51	2A8	1B7	1A4
67	I/O52	2A7	1B8	1A3
68	I/O53	2A4	1B11	1A2
69	I/O54	2A3	1B12	1A1
70	I/O55	2A2	1B13	1A0
71	GND			
72	V_{CC}			
73	I/O56	2B0	2A15	1B0
74	I/O57	2B1	2A14	1B1
75	I/O58	2B2	2A13	1B2
76	I/O59	2B3	2A12	1B3
77	I/O60	2B4	2A11	1B4
78	I/O61	2B5	2A10	1B5
79	I/O62	2B6	2A9	1B6
80	I/O63	2B7	2A8	1B7
81	GND			
82	I/O64	2B8	2A7	1B8
83	I/O65	2B9	2A6	1B9
84	I/O66	2B10	2A5	1B10
85	I/O67	2B11	2A4	1B11
86	I/O68	2B12	2A3	1B12
87	I/O69	2B13	2A2	1B13
88	V_{CC}			
89	GND			
90	GND			
91	GND			
92	GND			
93	V_{CC}			
94	I/O70	3B13	2B2	2B13
95	I/O71	3B12	2B3	2B12
96	I/O72	3B11	2B4	2B11
97	I/O73	3B10	2B5	2B10
98	I/O74	3B9	2B6	2B9
99	I/O75	3B8	2B7	2B8
100	GND			
101	I/O76	3B7	2B8	2B7
102	I/O77	3B6	2B9	2B6
103	I/O78	3B5	2B10	2B5
104	I/O79	3B4	2B11	2B4
105	I/O80	3B3	2B12	2B3
106	I/O81	3B2	2B13	2B2
107	I/O82	3B1	2B14	2B1
108	I/O83	3B0	2B15	2B0
109	V_{CC}			
110	GND			
111	I/O84	3A2	3B13	2A0
112	I/O85	3A3	3B12	2A1
113	I/O86	3A4	3B11	2A2
114	I/O87	3A7	3B8	2A3
115	I/O88	3A8	3B7	2A4
116	I/O89	3A11	3B4	2A5
117	I/O90	3A12	3B3	2A6
118	I/O91	3A13	3B2	2A7
119	V_{CC}			
120	GND			
121	TMS			
122	I/O92	4A2	3A2	2A8
123	I/O93	4A3	3A3	2A9
124	I/O94	4A4	3A4	2A10
125	I/O95	4A7	3A7	2A11
126	I/O96	4A8	3A8	2A12
127	I/O97	4A11	3A11	2A13
128	I/O98	4A12	3A12	2A14
129	I/O99	4A13	3A13	2A15
130	V_{CC}			
131	GND			
132	I/O100	4D15	3D15	2D15
133	I/O101	4D14	3D14	2D14
134	I/O102	4D13	3D13	2D13
135	I/O103	4D12	3D12	2D12
136	I/O104	4D11	3D11	2D11
137	I/O105	4D10	3D10	2D10
138	I/O106	4D9	3D9	2D9
139	I/O107	4D8	3D8	2D8
140	GND			
141	I/O108	4D7	3D7	2D7
142	I/O109	4D6	3D6	2D6
143	I/O110	4D5	3D5	2D5
144	I/O111	4D4	3D4	2D4
145	I/O112	4D3	3D3	2D3
146	I/O113	4D2	3D2	2D2
147	I/O114	4D1	3D1	2D1
148	I/O115	4D0	3D0	2D0
149	I2/CLK2			
150	V_{CC}			
151	GND			
152	I3/CLK3			
153	I/O116	5D0	4D0	3D0
154	I/O117	5D1	4D1	3D1
155	I/O118	5D2	4D2	3D2
156	I/O119	5D3	4D3	3D3
157	I/O120	5D4	4D4	3D4
158	I/O121	5D5	4D5	3D5
159	I/O122	5D6	4D6	3D6
160	I/O123	5D7	4D7	3D7
161	GND			
162	I/O124	5D8	4D8	3D8
163	I/O125	5D9	4D9	3D9
164	I/O126	5D10	4D10	3D10
165	I/O127	5D11	4D11	3D11
166	I/O128	5D12	4D12	3D12
167	I/O129	5D13	4D13	3D13
168	I/O130	5D14	4D14	3D14
169	I/O131	5D15	4D15	3D15
170	GND			
171	V_{CC}			
172	I/O132	5A13	4A13	3A13
173	I/O133	5A12	4A12	3A12
174	I/O134	5A11	4A11	3A11
175	I/O135	5A8	4A8	3A8
176	I/O136	5A7	4A7	3A7
177	I/O137	5A4	4A4	3A4
178	I/O138	5A3	4A3	3A3
179	I/O139	5A2	4A2	3A2
180	TDO			
181	GND			
182	V_{CC}			
183	I/O140	6A13	4B2	3B2
184	I/O141	6A12	4B3	3B3
155	I/O142	6A11	4B4	3B4
186	I/O143	6A8	4B7	3B7
187	I/O144	6A7	4B8	3B8
188	I/O145	6A4	4B11	3B11
189	I/O146	6A3	4B12	3B12
190	I/O147	6A2	4B13	3B13
191	GND			
192	V_{CC}			
193	I/O148	6B0	5B15	4B15
194	I/O149	6B1	5B14	4B14
195	I/O150	6B2	5B13	4B13
196	I/O151	6B3	5B12	4B12
197	I/O152	6B4	5B11	4B11
198	I/O153	6B5	5B10	4B10
199	I/O154	6B6	5B9	4B9
200	I/O155	6B7	5B8	4B8
201	GND			
202	I/O156	6B8	5B7	4B7
203	I/O157	9B9	5B6	4B6
204	I/O158	6B10	5B5	4B5
205	I/O159	6B11	5B4	4B4
206	I/O160	6B12	5B3	4B3
207	I/O161	6B13	5B2	4B2
208	V_{CC}			
209	GND			
210	GND			
211	GND			
212	GND			
213	V_{CC}			
214	I/O162	7B13	5A2	4A2
215	I/O163	7B12	5A3	4A3
216	I/O164	7B11	5A4	4A4
217	I/O165	7B10	5A5	4A5
218	I/O166	7B9	5A6	4A6
219	I/O167	7B8	5A7	4A7
220	GND			
221	I/O168	7B7	5A8	4A8
222	I/O169	7B6	5A9	4A9
223	I/O170	7B5	5A10	4A10
224	I/O171	7B4	5A11	4A11
225	I/O172	7B3	5A12	4A12
226	I/O173	7B2	5A13	4A13
227	I/O174	7B1	5A14	4A14
228	I/O175	7B0	5A15	4A15
229	V_{CC}			
230	GND			
231	I/O176	7A2	0B13	0B13
232	I/O177	7A3	0B12	0B12
233	I/O178	7A4	0B11	0B11
234	I/O179	7A7	0B8	0B8
235	I/O180	7A8	0B7	0B7
236	I/O181	7A11	0B4	0B4
237	I/O182	7A12	0B3	0B3
238	I/O183	7A13	0B2	0B2
239	V_{CC}			
240	GND			

*Package obsolete, contact factory.

20446G-025

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V_{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out





256-BALL BGA CONNECTION DIAGRAM — M5-320, M5LV-320*, M5-384*, M5LV-384*, M5-512*, M5LV-512*

Bottom View (I/O Pin-outs)

256-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
1	GND	GND	I/O181	I/O182	I/O183	GND	I/O184	GND	I/O185	I/O186	GND	I/O187	GND	I/O188	GND	I/O189	I/O190	I/O191	GND	GND	1
2	GND	I/O164	I/O165	I/O166	I/O167	I/O168	I/O169	I/O170	I/O171	I3/CLK3	I2/CLK2	I/O172	I/O173	I/O174	I/O175	I/O176	I/O177	I/O178	I/O179	I/O180	2
3	GND	I/O148	V_{CC}	I/O149	I/O150	I/O151	I/O152	I/O153	I/O154	I/O155	I/O156	I/O157	I/O158	I/O159	I/O160	I/O161	I/O162	V_{CC}	I/O163	GND	3
4	I/O134	I/O135	I/O136	V_{CC}	TDO	I/O137	V_{CC}	I/O138	I/O139	I/O140	I/O141	I/O142	I/O143	V_{CC}	I/O144	TMS	V_{CC}	I/O145	I/O146	I/O147	4
5	I/O128	I/O129	I/O130	V_{CC}													V_{CC}	I/O131	I/O132	I/O133	5
6	GND	I/O122	I/O123	I/O124													I/O125	I/O126	I/O127	GND	6
7	I/O116	I/O117	I/O118	V_{CC}													V_{CC}	I/O119	I/O120	I/O121	7
8	I/O108	I/O109	I/O110	I/O111													I/O112	I/O113	I/O114	I/O115	8
9	GND	I/O102	I/O103	I/O104													I/O105	I/O106	I/O107	GND	9
10	GND	I/O96	I/O97	I/O98													I/O99	I/O100	I/O101	GND	10
11	GND	I/O90	I/O91	I/O92													I/O93	I/O94	I/O95	GND	11
12	GND	I/O84	I/O85	I/O86													I/O87	I/O88	I/O89	GND	12
13	I/O76	I/O77	I/O78	I/O79													I/O80	I/O81	I/O82	I/O83	13
14	I/O70	I/O71	I/O72	V_{CC}													V_{CC}	I/O73	I/O74	I/O75	14
15	GND	I/O64	I/O65	I/O66													I/O67	I/O68	I/O69	GND	15
16	I/O58	I/O59	I/O60	V_{CC}													V_{CC}	I/O61	I/O62	I/O63	16
17	I/O44	I/O45	I/O46	V_{CC}	TDI	I/O47	V_{CC}	I/O48	I/O49	I/O50	I/O51	I/O52	I/O53	V_{CC}	I/O54	TCK	V_{CC}	I/O55	I/O56	I/O57	17
18	GND	I/O28	V_{CC}	I/O29	I/O30	I/O31	I/O32	I/O33	I/O34	I/O35	I/O36	I/O37	I/O38	I/O39	I/O40	I/O41	I/O42	V_{CC}	I/O43	GND	18
19	I/O11	I/O12	I/O13	I/O14	I/O15	I/O16	I/O17	I/O18	I/O19	IO/CLK0	I1/CLK1	I/O20	I/O21	I/O22	I/O23	I/O24	I/O25	I/O26	I/O27	GND	19
20	GND	GND	I/O0	I/O1	I/O2	GND	I/O3	GND	I/O4	GND	I/O5	I/O6	GND	I/O7	GND	I/O8	I/O9	I/O10	GND	GND	20
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V_{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

20446G-026

*Package obsolete, contact factory.



256-BALL BGA CONNECTION DIAGRAM — M5-320, M5LV-320*

Bottom View (Macrocell Association)

256-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
1	GND	GND	3A11	3D15	3D12	GND	3D7	GND	3D3	3D2	GND	2D2	GND	2D7	GND	2D10	2D13	2D15	GND	GND	1
2	GND	3B2	3A3	3A8	3A13	3D13	3D9	3D8	3D4	I3/CLK3	I2/CLK2	2D3	2D4	2D8	2D12	2A15	2A13	2A12	2A9	2A7	2
3	GND	3B8	V_{CC}	3A2	3A4	3A12	3D14	3D10	3D5	3D0	2D0	2D5	2D9	2D14	2A14	2A10	2A8	V_{CC}	2A3	GND	3
4	3B13	3B11	3B3	V_{CC}	TDO	3A7	V_{CC}	3D11	3D6	3D1	2D1	2D6	2D11	V_{CC}	2A11	TMS	V_{CC}	2A6	2A2	2A0	4
5	4B14	4B15	3B4	V_{CC}													V_{CC}	2A5	2B0	2B1	5
6	GND	4B11	3B12	3B7													2A4	2A1	2B4	GND	6
7	4B8	4B10	4B13	V_{CC}													V_{CC}	2B2	2B5	2B7	7
8	4B4	4B6	4B9	4B12													2B3	2B6	2B9	2B11	8
9	GND	4B3	4B5	4B7													2B8	2B10	2B12	GND	9
10	GND	4B0	4B1	4B2													2B13	2B14	2B15	GND	10
11	GND	4A0	4A1	4A2													1B13	1B14	1B15	GND	11
12	GND	4A3	4A5	4A7													1B8	1B10	1B12	GND	12
13	4A4	4A6	4A9	4A12													1B3	1B6	1B9	1B11	13
14	4A8	4A10	4A13	V_{CC}													V_{CC}	1B2	1B5	1B7	14
15	GND	4A11	0B12	0B7													1A4	1A1	1B4	GND	15
16	4A14	4A15	0B4	V_{CC}													V_{CC}	1A5	1B0	1B1	16
17	0B13	0B11	0B3	V_{CC}	TDI	0A7	V_{CC}	0D11	0D6	0D1	1D1	1D6	1D11	V_{CC}	1A11	TCK	V_{CC}	1A6	1A2	1A0	17
18	GND	0B8	V_{CC}	0A2	0A4	0A12	0D14	0D9	0D5	0D0	1D0	1D5	1D10	1D14	1A14	1A10	1A8	V_{CC}	1A3	GND	18
19	0B2	0A3	0A8	0A11	0A13	0D12	0D8	0D4	0D3	I0/CLK0	I1/CLK1	1D4	1D8	1D9	1D13	1A15	1A12	1A9	1A7	GND	19
20	GND	GND	0D15	0D13	0D10	GND	0D7	GND	0D2	GND	1D2	1D3	GND	1D7	GND	1D12	1D15	1A13	GND	GND	20
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

4 D 15
15 — Macrocell (0-15)
D — PAL Block (A-D)
4 — Segment (0-4)

*Package obsolete, contact factory.

20446G-029



256-BALL BGA CONNECTION DIAGRAM — M5-384*, M5LV-384*

Bottom View (Macrocell Association)

256-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
1	GND	GND	4A11	4D15	4D12	GND	4D7	GND	4D3	4D2	GND	3D2	GND	3D7	GND	3D10	3D13	3D15	GND	GND	1
2	GND	4B2	4A3	4A8	4A13	4D13	4D9	4D8	4D4	I3/CLK3	I2/CLK2	3D3	3D4	3D8	3D12	3A13	3A11	3A8	3A3	3B2	2
3	GND	4B8	V_{CC}	4A2	4A4	4A12	4D14	4D10	4D5	4D0	3D0	3D5	3D9	3D14	3A12	3A4	3A2	V_{CC}	3B8	GND	3
4	4B13	4B11	4B3	V_{CC}	TDO	4A7	V_{CC}	4D11	4D6	4D1	3D1	3D6	3D11	V_{CC}	3A7	TMS	V_{CC}	3B3	3B11	3B13	4
5	5B14	5B15	4B4	V_{CC}													V_{CC}	3B4	2B15	2B14	5
6	GND	5B11	4B12	4B7													3B7	3B12	2B11	GND	6
7	5B8	5B10	5B13	V_{CC}													V_{CC}	2B13	2B10	2B8	7
8	5B4	5B6	5B9	5B12													2B12	2B9	2B6	2B4	8
9	GND	5B3	5B5	5B7													2B7	2B5	2B3	GND	9
10	GND	5B0	5B1	5B2													2B2	2B1	2B0	GND	10
11	GND	5A0	5A1	5A2													2A2	2A1	2A0	GND	11
12	GND	5A3	5A5	5A7													2A7	2A5	2A3	GND	12
13	5A4	5A6	5A9	5A12													2A12	2A9	2A6	2A4	13
14	5A8	5A10	5A13	V_{CC}													V_{CC}	2A13	2A10	2A8	14
15	GND	5A11	0B12	0B7													1B7	1B12	2A11	GND	15
16	5A14	5A15	0B4	V_{CC}													V_{CC}	1B4	2A15	2A14	16
17	0B13	0B11	0B3	V_{CC}	TDI	0A7	V_{CC}	0D11	0D6	0D1	1D1	1D6	1D11	V_{CC}	1A7	TCK	V_{CC}	1B3	1B11	1B13	17
18	GND	0B8	V_{CC}	0A2	0A4	0A12	0D14	0D9	0D5	0D0	1D0	1D5	1D10	1D14	1A12	1A4	1A2	V_{CC}	1B8	GND	18
19	0B2	0A3	0A8	0A11	0A13	0D12	0D8	0D4	0D3	IO/CLK0	I1/CLK1	1D4	1D8	1D9	1D13	1A13	1A8	1A3	1B2	GND	19
20	GND	GND	0D15	0D13	0D10	GND	0D7	GND	0D2	GND	1D2	1D3	GND	1D7	GND	1D12	1D15	1A11	GND	GND	20
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V_{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

5 D 15

- 15 — Macrocell (0-15)
- D — PAL Block (A-D)
- 5 — Segment (0-5)

*Package obsolete, contact factory.

20446G-028



256-BALL BGA CONNECTION DIAGRAM — M5-512*, M5LV-512*

Bottom View (Macrocell Association)

256-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
1	GND	GND	5A11	5D15	5D12	GND	5D7	GND	5D3	5D2	GND	4D2	GND	4D7	GND	4D10	4D13	4D15	GND	GND	1
2	GND	6A13	5A3	5A8	5A13	5D13	5D9	5D8	5D4	I3/CLK3	I2/CLK2	4D3	4D4	4D8	4D12	4A13	4A11	4A8	4A3	3A13	2
3	GND	6A7	V_{CC}	5A2	5A4	5A12	5D14	5D10	5D5	5D0	4D0	4D5	4D9	4D14	4A12	4A4	4A2	V_{CC}	3A7	GND	3
4	6A2	6A4	6A12	V_{CC}	TDO	5A7	V_{CC}	5D11	5D6	5D1	4D1	4D6	4D11	V_{CC}	4A7	TMS	V_{CC}	3A12	3A4	3A2	4
5	6B1	6B0	6A11	V_{CC}													V_{CC}	3A11	3B0	3B1	5
6	GND	6B4	6A3	6A8													3A8	3A3	3B4	GND	6
7	6B7	6B5	6B2	V_{CC}													V_{CC}	3B2	3B5	3B7	7
8	6B11	6B9	6B6	6B3													3B3	3B6	3B9	3B11	8
9	GND	6B12	6B10	6B8													3B8	3B10	3B12	GND	9
10	GND	6B15	6B14	6B13													3B13	3B14	3B15	GND	10
11	GND	7B15	7B14	7B13													2B13	2B14	2B15	GND	11
12	GND	7B12	7B10	7B8													2B8	2B10	2B12	GND	12
13	7B11	7B9	7B6	7B3													2B3	2B6	2B9	2B11	13
14	7B7	7B5	7B2	V_{CC}													V_{CC}	2B2	2B5	2B7	14
15	GND	7B4	7A3	7A8													2A8	2A3	2B4	GND	15
16	7B1	7B0	7A11	V_{CC}													V_{CC}	2A11	2B0	2B1	16
17	7A2	7A4	7A12	V_{CC}	TDI	0A7	V_{CC}	0D11	0D6	0D1	1D1	1D6	1D11	V_{CC}	1A7	TCK	V_{CC}	2A12	2A4	2A2	17
18	GND	7A7	V_{CC}	0A2	0A4	0A12	0D14	0D9	0D5	0D0	1D0	1D5	1D10	1D14	1A12	1A4	1A2	V_{CC}	2A7	GND	18
19	7A13	0A3	0A8	0A11	0A13	0D12	0D8	0D4	0D3	IO/CLK0	I1/CLK1	1D4	1D8	1D9	1D13	1A13	1A8	1A3	2A13	GND	19
20	GND	GND	0D15	0D13	0D10	GND	0D7	GND	0D2	GND	1D2	1D3	GND	1D7	GND	1D12	1D15	1A11	GND	GND	20
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

5 D 15
- 15 — Macrocell (0-15)
- D — PAL Block (A-D)
- 5 — Segment (0-5)

20446G-027

*Package obsolete, contact factory.



352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

Bottom View (I/O Pin-outs)

352-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF
1	NC	NC	NC	GND	NC	I/O245	GND	I/O246	I/O247	GND	I/O248	I/O249	I3/CLK3	GND	I/O250	I/O251	I/O252	GND	I/O253	I/O254	GND	NC	I/O255	GND	NC	NC
2	NC	NC	NC	I/O224	I/O225	I/O226	I/O227	I/O228	I/O229	I/O230	I/O231	I/O232	I/O233	I/O234	I/O235	I/O236	I/O237	I/O238	I/O239	I/O240	I/O241	I/O242	I/O243	I/O244	GND	GND
3	GND	GND	NC	I/O205	I/O206	I/O207	I/O208	I/O209	I/O210	I/O211	I/O212	I/O213	I/O214	I2CLK2	I/O215	I/O216	I/O217	I/O218	I/O219	I/O220	I/O221	I/O222	I/O223	TMS	NC	NC
4	NC	I/O188	NC	TDO	I/O189	I/O190	I/O191	V_{CC}	I/O192	V_{CC}	I/O193	I/O194	I/O195	V_{CC}	I/O196	I/O197	I/O198	V_{CC}	I/O199	V_{CC}	I/O200	I/O201	V_{CC}	I/O202	I/O203	I/O204
5	GND	I/O183	I/O184	V_{CC}																			I/O185	I/O186	I/O187	GND
6	NC	I/O176	I/O177	I/O178																			I/O179	I/O180	I/O181	I/O182
7	GND	I/O169	I/O170	I/O171																			I/O172	I/O173	I/O174	I/O175
8	I/O162	I/O163	I/O164	I/O165																			I/O166	I/O167	I/O168	NC
9	I/O156	I/O157	I/O158	I/O159																			V_{CC}	I/O160	I/O161	GND
10	GND	I/O150	I/O151	V_{CC}																			I/O152	I/O153	I/O154	I/O155
11	I/O142	I/O143	I/O144	I/O145																			I/O146	I/O147	I/O148	I/O149
12	I/O134	I/O135	I/O136	I/O137																			I/O138	I/O139	I/O140	I/O141
13	I/O128	I/O129	I/O130	I/O131																			V_{CC}	I/O132	I/O133	GND
14	GND	I/O122	I/O123	V_{CC}																			I/O124	I/O125	I/O126	I/O127
15	I/O114	I/O115	I/O116	I/O117																			I/O118	I/O119	I/O120	I/O121
16	NC	I/O107	I/O108	I/O109																			I/O110	I/O111	I/O112	I/O113
17	I/O101	I/O102	I/O103	I/O104																			V_{CC}	I/O105	I/O106	GND
18	GND	I/O95	I/O96	V_{CC}																			I/O97	I/O98	I/O99	I/O100
19	I/O87	I/O88	I/O89	I/O90																			I/O91	I/O92	I/O93	I/O94
20	I/O80	I/O81	I/O82	I/O83																			I/O84	I/O85	I/O86	GND
21	I/O73	I/O74	I/O75	I/O76																			I/O77	I/O78	I/O79	NC
22	GND	I/O68	I/O69	I/O70																			V_{CC}	I/O71	I/O72	GND
23	I/O51	I/O52	I/O53	V_{CC}	I/O54	I/O55	V_{CC}	I/O56	V_{CC}	I/O57	I/O58	I/O59	V_{CC}	I/O60	I/O61	I/O62	V_{CC}	I/O63	V_{CC}	I/O64	I/O65	I/O66	TCK	NC	I/O67	NC
24	NC	NC	TDI	I/O32	I/O33	I/O34	I/O35	I/O36	I/O37	I/O38	I/O39	I/O40	I0/CLK0	I/O41	I/O42	I/O43	I/O44	I/O45	I/O46	I/O47	I/O48	I/O49	I/O50	NC	GND	GND
25	GND	GND	I/O11	I/O12	I/O13	I/O14	I/O15	I/O16	I/O17	I/O18	I/O19	I/O20	I/O21	I/O22	I/O23	I/O24	I/O25	I/O26	I/O27	I/O28	I/O29	I/O30	I/O31	NC	NC	NC
26	NC	NC	GND	I/O0	NC	GND	I/O1	I/O2	GND	I/O3	I/O4	I/O5	GND	I1/CLK1	I/O6	I/O7	GND	I/O8	I/O9	GND	I/O10	NC	GND	NC	NC	NC

Pin Designations

CLK	=	Clock
GND	=	Ground
I	=	Input
I/O	=	Input/Output
NC	=	No Connect
V_{CC}	=	Supply Voltage
TDI	=	Test Data In
TCK	=	Test Clock
TMS	=	Test Mode Select
TDO	=	Test Data Out

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352-BALL BGA CONNECTION DIAGRAM — M5-512, M5LV-512

Bottom View (I/O Pin-outs)

352-Ball BGA

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	AF	
1	NC	NC	NC	GND	NC	5A12	GND	5D15	5D11	GND	5D6	5D3	I3/CLK3	GND	4D1	4D5	4D9	GND	4D15	4A13	GND	NC	4A6	GND	NC	NC	1
2	NC	NC	NC	5A2	5A5	5A9	5A14	5A15	5D13	5D10	5D8	5D4	5D0	4D0	4D2	4D6	4D10	4D13	4A15	4A12	4A9	4A8	4A3	4A1	GND	GND	2
3	GND	GND	NC	5A1	5A4	5A7	5A8	5A10	5A13	5D14	5D9	5D5	5D1	I2/CLK2	4D4	4D7	4D11	4D14	4A14	4A10	4A7	4A5	4A2	TMS	NC	NC	3
4	NC	6A14	NC	TDO	5A0	5A3	5A6	V_{CC}	5A11	V_{CC}	5D12	5D7	5D2	V_{CC}	4D3	4D8	4D12	V_{CC}	4A11	V_{CC}	4A4	4A0	V_{CC}	3A15	3A13	3A12	4
5	GND	6A12	6A13	V_{CC}																			3A14	3A11	3A9	GND	5
6	NC	6A9	6A10	6A15																			3A10	3A8	3A7	3A5	6
7	GND	6A6	6A8	6A11																			3A6	3A4	3A3	3A0	7
8	6A1	6A4	6A5	6A7																			3A2	3A1	3B0	NC	8
9	6B1	6A0	6A2	6A3																			V_{CC}	3B1	3B2	GND	9
10	GND	6B2	6B0	V_{CC}																			3B3	3B4	3B5	3B6	10
11	6B6	6B5	6B4	6B3																			3B7	3B8	3B9	3B10	11
12	6B10	6B9	6B8	6B7																			3B11	3B12	3B13	3B14	12
13	6B14	6B13	6B12	6B11																			V_{CC}	2B15	3B15	GND	13
14	GND	7B15	6B15	V_{CC}																			2B11	2B12	2B13	2B14	14
15	7B14	7B13	7B12	7B11																			2B7	2B8	2B9	2B10	15
16	NC	7B10	7B9	7B8																			2B3	2B4	2B5	2B6	16
17	7B7	7B6	7B5	7B4																			V_{CC}	2B0	2B2	GND	17
18	GND	7B3	7B2	V_{CC}																			2A3	2A2	2A0	2B1	18
19	7B1	7B0	7A1	7A4																			2A7	2A5	2A4	2A1	19
20	7A0	7A2	7A3	7A8																			2A11	2A8	2A6	GND	20
21	7A5	7A6	7A7	7A12																			2A15	2A10	2A9	NC	21
22	GND	7A9	7A11	7A15																			V_{CC}	2A13	2A12	GND	22
23	7A10	7A13	7A14	V_{CC}	0A0	0A4	V_{CC}	0A11	V_{CC}	0D12	0D8	0D3	V_{CC}	1D2	1D7	1D12	V_{CC}	1A11	V_{CC}	1A6	1A3	1A0	TCK	NC	2A14	NC	23
24	NC	NC	TDI	0A2	0A5	0A7	0A10	0A14	0D14	0D11	0D7	0D4	I0/CLK0	1D1	1D5	1D9	1D14	1A13	1A10	1A8	1A7	1A4	1A1	NC	GND	GND	24
25	GND	GND	0A1	0A3	0A8	0A9	0A12	0A15	0D13	0D10	0D6	0D2	0D0	1D0	1D4	1D8	1D10	1D13	1A15	1A14	1A9	1A5	1A2	NC	NC	NC	25
26	NC	NC	GND	0A6	NC	GND	0A13	0D15	GND	0D9	0D5	0D1	GND	I1/CLK1	1D3	1D6	GND	1D11	1D15	GND	1A12	NC	GND	NC	NC	NC	26
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	D	AE	AF	

Pin Designations

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
V_{CC} = Supply Voltage
TDI = Test Data In
TCK = Test Clock
TMS = Test Mode Select
TDO = Test Data Out

7 D 15

15 — Macrocell (0-15)
D — PAL Block (A-D)
7 — Segment (0-7)

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5V M5 ORDERING INFORMATION[1,2]

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.

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M5- 512 /256 -7 A C

FAMILY TYPE
M5- = MACH 5 (5-V V_{CC})

MACROCELL DENSITY
128 = 128 Macrocells
192 = 192 Macrocells
256 = 256 Macrocells
320 = 320 Macrocells
384 = 384 Macrocells
512 = 512 Macrocells

I/Os
/68 = 68 I/Os in 100-pin PQFP or TQFP
/74 = 74 I/Os in 100-pin TQFP
/104 = 104 I/Os in 144-pin PQFP or TQFP
/120 = 120 I/Os in 160-pin PQFP
/160 = 160 I/Os in 208-pin PQFP
/192 = 192 I/Os in 256-ball BGA
/256 = 256 I/Os in 352-ball BGA

PROGRAMMING DESIGNATOR
Blank = Initial Algorithm
/1 = First Revision

OPERATING CONDITIONS
C = Commercial (0°C to +70°C)
I = Industrial (-40°C to +85°C)

PACKAGE TYPE
Y = Plastic Quad Flat Pack (PQFP)
V = Thin Quad Flat Pack (TQFP)
A = Ball Grid Array (BGA)
H = Plastic Quad Flat Pack (PQFP) with exposed heat sink

SPEED
-5 = 5.5 ns t_{PD}
-6 = 6.5 ns t_{PD}
-7 = 7.5 ns t_{PD}
-10 = 10 ns t_{PD}
-12 = 12 ns t_{PD}
-15 = 15 ns t_{PD}
-20 = 20 ns t_{PD}

Note:
1. See below for valid device/package combinations.
2. M5-128/1, M5-192/1 and M5-256/1 recommended for new designs.

Valid Combinations		
M5-128/68	Commercial: -5, -7, -10, -12, -15 Industrial: -7, -10, -12, -15, -20	YC, VC, YI, VI
M5-128/104		YC, YI
M5-128/120		YC, YI
M5-192/68		YC*, VC, YI*, VI
M5-192/104		YC*, YI*
M5-192/120		YC, YI
M5-256/68		YC*, VC, YI*, VI
M5-256/104		YC*, YI*
M5-256/120		YC, YI
M5-256/160		YC, YI

*Package obsolete, contact factory.

** Contact Factory for availability.

Valid Combinations		
M5-320/120	Commercial: -6, -7, -10, -12, -15 Industrial: -7, -10, -12, -15, -20	HC*, HI*
M5-320/160		HC, YC**, HI, YI**
M5-320/184		HC*, HI*
M5-320/192		AC, AI
M5-384/120		HC*, HI*
M5-384/160		HC, YC**, HI, YI**
M5-384/184		HC*, HI*
M5-384/192		AC*, AI*
M5-512/120		HC*, HI*
M5-512/160		HC, YC**, HI, YI**
M5-512/184		HC*, HI*
M5-512/192		AC*, AI*
M5-512/256		AC, AI

Device Marking

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5-512/256-7AC-10AI.

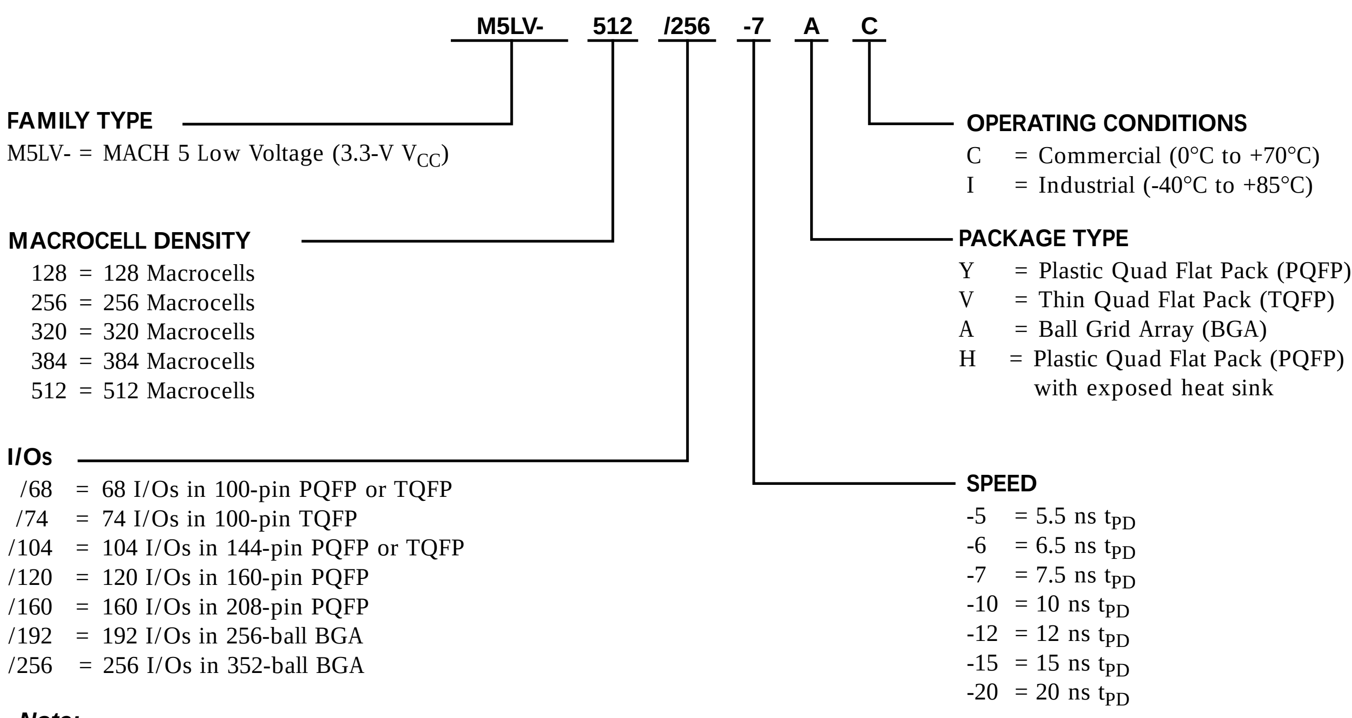
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.



3.3V M5LV ORDERING INFORMATION[1]

Lattice standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the elements below.



Note:
1. See below for valid device/package combinations.

Valid Combinations		
M5LV-128/68	Commercial: -5, -7, -10, -12 Industrial: -7, -10, -12, -15	YC*, VC, YI*, VI
M5LV-128/74		VC, VI
M5LV-128/104		YC*, VC, YI*, VI
M5LV-128/120		YC, YI
M5LV-256/68		YC, VC*, YI, VI*
M5LV-256/74		VC, VI
M5LV-256/104		YC*, VC, YI*, VI
M5LV-256/120		YC, YI
M5LV-256/160		YC, YI

*Package obsolete, contact factory.

** Contact Factory for availability.

Device Marking

Actual device marking differs from the ordering part number (OPN). All MACH devices are dual-marked with both Commercial and Industrial grades. The Industrial grade is slower, i.e., M5LV-512/256-7AC-10AI.

Valid Combinations		
M5LV-320/120	Commercial: -6, -7, -10, -12, -15 Industrial: -10, -12, -15, -20	HC, YC**, HI, YI**
M5LV-320/160		HC, YC**, HI, YI**
M5LV-320/184		HC*, HI*
M5LV-320/192		AC*, AI*
M5LV-384/120		HC, YC**, HI, YI**
M5LV-384/160		HC, YC**, HI, YI**
M5LV-384/184		HC*, HI*
M5LV-384/192		AC*, AI*
M5LV-512/120		HC, YC**, HI, YI**
M5LV-512/160		HC, YC**, HI, YI**
M5LV-512/184		HC*, HI*
M5LV-512/192		AC*, AI*
M5LV-512/256		AC, AI

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local Lattice sales office to confirm availability of specific valid combinations and to check on newly released combinations.